ATARI® FALCON030™ Service Guide
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Table of Contents

Section One: Introduction 1
1.0 Overview 1
1.1 System Features 1
1.2 Case Design 2
1.2.1 Front View 2
1.2.2 Rear View 2
1.2.3 Left Side View 3
1.2.4 Right Side View 3
1.2.5 Bottom View 3
1.3 Power Supply 4
1.3.1 Specifications 4
1.3.1.1 AC Input 4
1.3.1.2 DC Output 4
1.3.1.3 Operational Characteristics 5
Section Two: Theory of Operation 7
2.0 Overview 7
2.1 Main System 7
2.1.1 MC68030FG Microprocessor 7
2.1.1.1 MC68030FG Pin and Signal Description 8
2.1.2 MC68882 Optional Coprocessor 10
2.1.2.1 MC68882 Pin List and Signal Description 10
2.1.3 ROM 11
2.1.4 System RAM 12
2.1.4.1 System RAM Connector Pin List 13
2.1.4.1.1 50-Pin Connector J17 13
2.1.4.1.2 30-Pin Connector J6 14
2.1.4.2 System Memeory Map 14
2.1.5 COMBO IC 15
2.1.5.1 Memory Control Unit 15
2.1.5.2 Interrupt Mask and Status Control 15
2.1.5.2.1 Interrupt Priority Level Signal Definition 16
2.1.5.3 Buss Error Circuitry and Illegal Condition Detect 16
2.1.5.4 Clock Dividers 16
2.1.5.5 Chip Selects 16
2.1.5.6 Paddle Circuitry 16
2.1.5.7 Joystick Circuitry 16
2.1.5.8 Blitter 17
2.1.5.9 Light Gun Circuitry 17
2.1.5.10 COMBO IC Pin List and Signal Description 17
2.1.6 DMA Support 20
2.1.6.1 DMA Pin and Signal List 21
2.1.7 Real-Time Clock 24
2.1.7.1 Real-Time Clock Pin and Signal List 25
2.1.8 System Timing and Bus Control 25
2.1.8.1 68000 Bus Decode PAL U68 26
2.1.8.2 68000 Bus Decode PAL U63 26
2.1.8.3 68000 Bus Decode PAL U62 26
2.1.8.4 68000 Bus Decode PAL U67 26
2.1.8.5 68000 Bus Decode GAL U44 26
2.1.9 Configuration Switch 27
2.2 Audio/Video Subsystem 28
2.2.1 Video Subsystem Overview 28

2.2.1.1 Video RAM 29
2.2.1.2 Interrupt and Data Load Control (COMBO) 29
2.2.1.3 Video Shifter (VIDEL) 30
2.2.1.4 Video to Digital Analog Converter (SGC DAC) 30
2.2.1.4.1 Video to Digital Analog Converter Pin and Signal List 31
2.2.1.5 NTSC/PAL Encoder (1377) 31
2.2.1.6 VIDEL Pin and Signal List 33
2.2.1.7 Monitor Connector Pin List 33
2.2.2 Audio Subsystem 33
2.2.2.1 Prigrammable Sound Generator 33
2.2.2.2 DMA Sound 34
2.2.2.3 CODEC IC 34
2.2.2.3.1 CODEC Pin and Signal List 34
2.3 I/O Subsystems 37
2.3.1 SCSI II Interface 37
2.3.1.1 5380 SCSI Controller Pin and Signal List 37
2.3.1.2 External SCSI Connector Pin List 39
2.3.2 Floppy Disk (FDD) 39
2.3.2.1 AJAX Pin and Signal List 40
2.3.2.2 Internal Floppy Connector Pin List 41
2.3.3 68901 MFP 42
2.3.3.1 Interrupt Control 42
2.3.3.2 68901 MFP Pin and Signal List 42
2.3.4 8530 Serial Communications Controller (SCC) 44
2.3.4.1 8530 Pin and Signal List 45
2.3.4.2 Serial Port Pin and Signal List 48
2.3.4.3 SCC LAN Connector Pinout 48
2.3.5 Parallel Printer Port 48
2.3.5.1 Parallel Port Connector Pin List 49
2.3.6 Keyboard Interface 50
2.3.7 Mouse and Joystick Interface 50
2.3.7.1 Mouse and Joystick Interface Connector Pin List 50
2.3.8 Game Controller Ports 51
2.3.8.1 Game Controller Pinout 51
2.3.9 ROM Cartridge 52
2.3.9.1 ROM Cartridge Connector Pin List 53
2.3.10 Musical Instrument Digital Interface (MIDI) 53
2.3.10.1 MIDI Connector Pin List 54
2.3.11 Digital Processor Interface (DSP) 55
2.3.11.1 DSP Pin and Signal List 55
2.3.11.2 DSP Connector Pin List 57
2.3.12 IDE Interface 57
2.3.12.1 IDE Connector Pin List 58
2.3.13 Expansion Connector 58
2.3.13.1 Expansion Connector Pin List 59
2.4 System Startup 61
2.5 System Errors 61
2.5.1 Number of Bombs and Meaning 62
2.6 Overall Block Diagram 63
Section Three: Testing 65
3.0 Overview 65
3.1 Test Equipment 66
3.2 Test Configuration 66

3.3 Troubleshooting a Dead Unit 68
3.4 FALCON030 Diagnostic Cartridge 68
3.5 Power Up Sequence 69
3.5.1 Initialization and Check Sequence 69
3.5.1.1 RAM 69
3.5.1.1.1 All Ones - All Zeros (I1) 69
3.5.1.1.2 Walking Zeros (I1) 69
3.5.1.1.3 Address Line Shorting (I2) 69
3.5.1.1.4 Low 2K RAM Address Check (I3) 69
3.5.1.1.5 RAM Stack Test 69
3.5.1.2 System Initialization 70
3.5.1.3 Check Messages 70
3.5.1.3.1 Bus Error Check 70
3.5.1.3.2 FPU Check 70
3.5.1.3.3 FALCON Specific Checks 70
3.5.1.3.4 PSG and Printer Port Initialization 70
3.5.1.3.5 Timer Testing - GENLOCK 70
3.5.1.4 Clean Up 71
3.5.2 Error Message Summary 71
3.5.2.1 Initialization Errors 71
3.5.2.2 Check Message Summary 72
3.6 Test Menu 72
3.6.1 Diagnostic Tests Menu 73
3.6.2 Main Menu Test Selection 73
3.6.2.1 Unattended Tests 73
3.6.2.1.1 RAM & SRAM Test 74
3.6.2.1.2 ROM Test 74
3.6.1.2.3 MIDI Tests 75
3.6.1.2.4 SCC Serial Port 75
3.6.1.2.5 Timing 75
3.6.1.2.6 SCSI DMA 76
3.6.1.2.7 Floppy Disk 77
3.6.1.2.8 Printer/Joy/Game 79
3.6.1.2.9 Real-Time Clock 81
3.6.1.2.10 Short BLiT 82
3.6.1.2.11 Long BLiT 82
3.6.1.2.12 Expansion Port 83
3.6.2.2 Operator Tests 85
3.6.2.2.1 Audio 85
3.6.2.2.1.1 PSG Sound 85
3.6.2.2.1.2 1kHz Mono Tone 85
3.6.2.2.1.3 1kHz/500 Hz Stereo Tones 85
3.6.2.2.1.4 Treble Attenuation 85
3.6.2.2.1.5 Bass Attenuation 85
3.6.2.2.2 Video 86
3.6.2.2.2.1 Color Test 86
3.6.2.2.2.2 Video Monitors Test 86
3.6.2.2.2.3 VGA Modes Test 88
3.6.2.2.3 Keyboard 89
3.6.2.2.4 IDE Hard Disk 89
3.7 Error Codes Quick Reference 91
Section Four: Disassembly/Assembly 99
4.1 FALCON030 Disassembly 99

4.1.1 Top Cover/Keyboard Removal 99
4.1.2 Shield and Speaker Removal 99
4.1.3 Floppy Disk Removal 99
4.1.4 Power Supply Removal 100
4.1.5 Memeory Board Removal 100
4.1.6 Removal of Main Assembly from Bottom Case 100
4.1.7 Removal of Upper Shield from Printed Circuit Board 100
4.2 FALCON030 Re-assembly 100
Section Five: Symptom Checklist 103
5.1 Display Problems 103
5.2 Disk Drive Problems 104
5.3 Keyboard {roblems 104
5.4 MIDI Problems 104
5.5 RS232 Problems 104
5.6 Printer Port Problems 104
5.7 Hard Disk Port Problems 105
5.8 DMA Sound 105
Section Six: Diagnostic Flowcharts 107
Section Seven: Parts List and Assembly Drawings 111
Section Eight: Glossary 127
Section Nine: Schematic and PCB Layout 131

SECTION ONE
INTRODUCTION

1.0 OVERVIEW

The latest enhancement to the Atari® ST™ architecture is the Atari FALCON030™ system. The system is comprised of an integrated housing which contains the CPU, System RAM, Floppy Disk, Optional Hard Disk, modular keyboard, and Power supply. A detachable mouse is also included. The system is compatible with previous designs including the STE™, and MEGA STE™.

The basic system is shipped with 1, 4, or 14 Mbytes of RAM, 512 Kbytes of ROM, 2 Mbyte (unformatted) Floppy Disk Drive, and high speed Motorola® MC68030FG™ CPU running at 16 MHz. FALCON030 also offers system expansion via an internal expansion connector.

1.1 SYSTEM FEATURES

Basic system features contained in the FALCON030 are as follows:

- MC68030FG Microprocessor running at 16 MHz
- Optional MC68881/MC68882 Coprocessor running at 16 MHz
- 1, 4, or 14 MB RAM
- 512 KB ROM
- Graphics Coprocessor (Blitter)
- ST™, VGA, True Color, and Programmable Video Modes
- Digital stereo sound
- Digital Signal Processor
- Parallel Port
- One RS232 Port
- MIDI Interface
- Cartridge Port
- External SCSI II DMA Port
- STE Compatible Joystick ports
- LAN Port
- 3½" 2 Mbyte Floppy Drive (unformatted)
- Internal Optional IDE Hard Disk
- 100 DPI Mouse
- Real-Time Clock
- Expansion Port

1.2 CASE DESIGN

1.2.1 FRONT VIEW

The front of the FALCON030 system includes LEDs for power, floppy disk access, and if an optional hard disk is installed, hard disk access. See Figure 1.

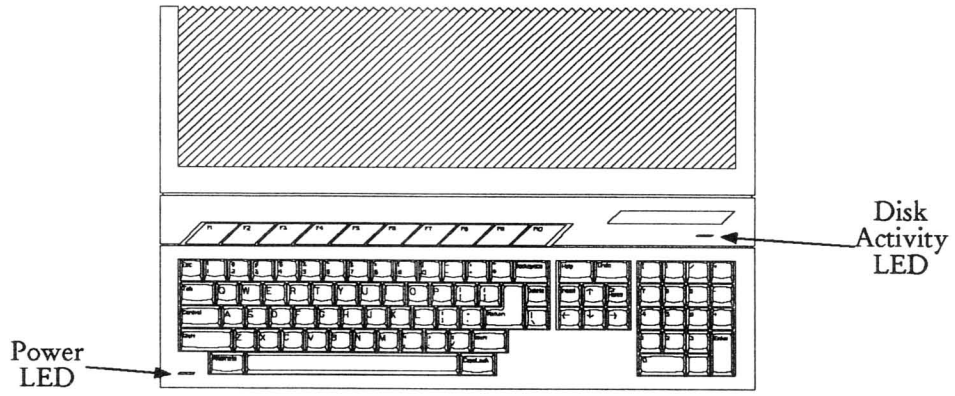


Figure 1

1.2.2 REAR VIEW

The rear of the FALCON030 system contains connectors for the digital audio interface, stereo jacks, SCSI II connector, monitor out/genlock, RF out, parallel port, serial port, LAN, reset button, on/off switch, and AC input. See Figure 2.

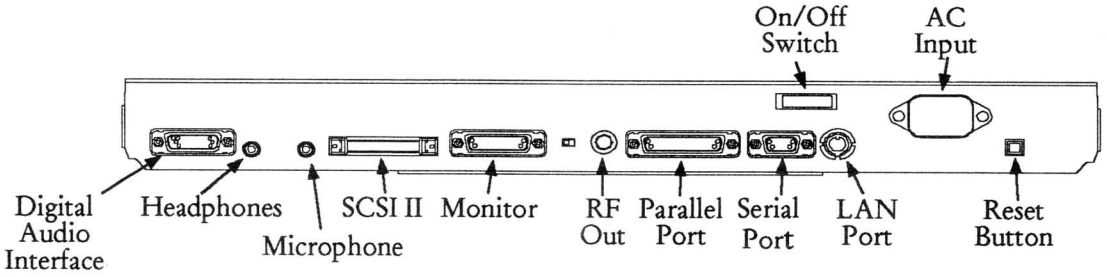


Figure 2

1.2.3 LEFT SIDE VIEW

The left side of the FALCON030 contains the cartridge port and game ports A and B. See Figure 3.

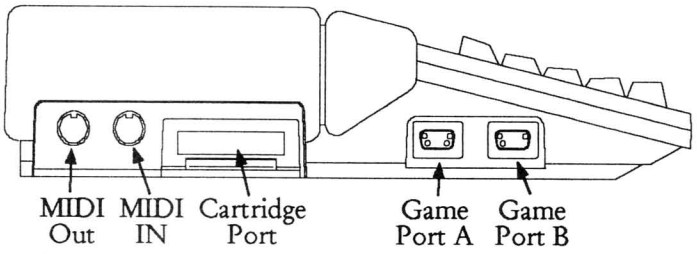


Figure 3

1.2.4 RIGHT SIDE VIEW

The right side of the FALCON030 contains the Floppy Disk Drive. See Figure 4.

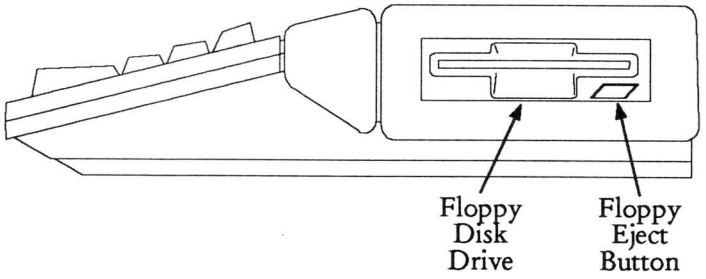


Figure 4

1.2.5 Bottom View

The bottom of the FALCON030 contains the Mouse/Joystick and Joystick connectors. See Figure 5.

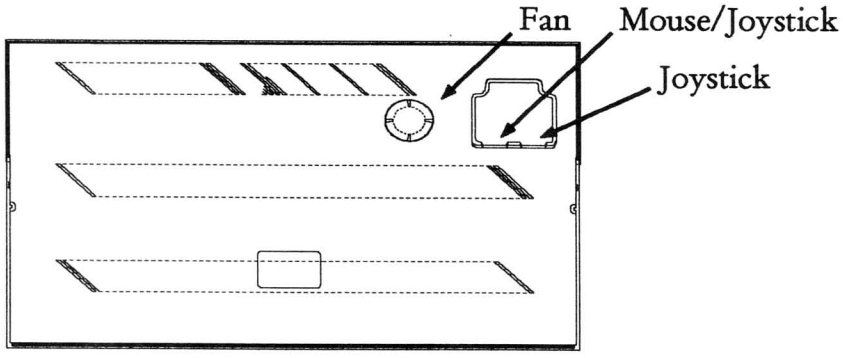


Figure 5

1.3 POWER SUPPLY

The system includes a switching power supply which is configured for 110 volt AC input US or 220/240 volt AC input European. The power supply provides 37.4 watts of power to the system. Voltages of +12V and +5V are provided to the main logic board as well as voltages for the floppy drive and optional hard disk.

1.3.1 SPECIFICATIONS

1.3.1.1 AC Input

Input	Country	
	U.S.	Europe
Voltage:	90 to 129 VAC (RMS) 117 VAC Nominal	198 to 264 VAC (RMS) 230 VAC Nominal
Frequency:	55 to 65 Hz	45 to 55 Hz
Current:	0.9 Amperes (RMS)	0.45 Amperes (RMS)
Maximum Inrush Current:	35 Amperes	35 Amperes

1.3.1.2 DC Output

Output	Voltage	
Voltage:	+5 VDC	+12 VDC
Minimum Load Current:	1.5 Amp	0.0 Amp
Maximum Load Current:	7.0 Amp	0.2 Amp
Line Regulation:	5%	10%
Load Regulation:	5%	10%
Cross Regulation:	5%	10%
Ripple:	100 millivolts p-p	100 millivolts p-p
Noise:	100 millivolts p-p	100 millivolts p-p

1.3.1.3 Operational Characteristics

Output	Characteristic
Peak Current:	+5 VDC peak current of 10 amperes for not more than 10 seconds with +12 VDC output at full load.
+5 VDC Set Point:	The +5 VDC output must be set to +5.05 0.1 VDC with a +5 VDC output having a load of 4.0 amperes.
Total Output Power:	37.4 watts
Efficiency:	55% minimum at full load, minimum frequency.
Hold Up Time:	10 milliseconds at 100% load and nominal input voltage.
Switching Frequency:	20 KHZ (minimum)
Temperature Coefficient:	0.04% per degree Centigrade
Power On Delay Time:	150 milliseconds (maximum)
Short Circuit Protection:	The power supply should switch off within 20 milliseconds
Overshoot:	(5% of the nominal output voltage) at turn on and off with the outputs not exceeding the limit.
Operating Temperature:	0 to +50 degrees Centigrade
Operating Humidity:	20% to 90% Relative Humidity
Operating Altitude:	0 to 3000 meters

SECTION TWO
THEORY OF OPERATION

2.0 OVERVIEW

The section discusses in general the components which make up the FALCON030 system and how they interrelate with one another. This will give you a basic working knowledge of the system's architecture necessary to repair most hardware failures which may occur. Other sections are provided in this manual to aid in use of diagnostics and troubleshooting techniques. The system is divided into three main categories. Main system, Audio/Video Subsystem, and I/O Subsystem. Each category will be covered separately along with any other components that may lie outside that section as it relates to that section's function within the system.

2.1 MAIN SYSTEM

The components which make up the main system are as follows:

- Motorola MC68030FG Microprocessor
- Optional Motorola MC68881/MC68882 Coprocessor
- 512 Kbyte ROM
- 1, 4, 14 Mbytes RAM
- COMBO IC
  - Memory Control Unit (MCU)
  - Clock Dividers
  - Interrupt Priority and Illegal Condition Detection
  - Chip Selects
  - Paddle Circuitry
  - Joystick Circuitry
  - Light Gun Circuitry
  - BLITTER
- DMA Support (SDMA IC)
- Real-Time Clock (1287 IC)
- System Timing and Bus Control (SDMA)
- Configuration Switch (S56, S57)

2.1.1 MC68030 Microprocessor

The Motorola MC68030FG is a 32-bit enhanced microprocessor which contains a central processing unit (CPU), enhanced bus controller, 256 byte instruction and data caches, and a memory management unit (MMU). The microprocessor is operated at 16 MHz.

The MC68030FG implements sixteen 32-bit general purpose data registers, two 32-bit supervisor stack pointers, ten special purpose control registers, and separate 32-bit non multiplexed address and data bus.

2.1.1.1 MC68030FG Pin List and Signal Description

General Function			
Pin	**Signal**	**Type**	**Description**
12,10,9	FC0-FC2	Output	3-bit function code used to identify the address space of each bus cycle.
21-22,58-58,33-31,29-26,36,24-23,56-51,48	A0-A31	Output	32-bit address bus.
75-76,78-83,86-89,91-94,96-99,101-104,106-109,11-114	D0-D31	I/O	32-bit data bus.
120,119	SIZ0-SIZ1	Output	Transfer Size bits indicate the number of bytes remaining to be transferred for the current bus cycle. These signals together with A0 and A1 define the active sections of the data bus.
Bus Control Signals			
Pin	**Signal**	**Type**	**Description**
117	R/(W)-	Output	Read/Write- indicates whether the current bus cycle is a read or write cycle. When low it indicates a write cycle, when high it indicates a read cycle.
124	DS-	Output	Data Strobe indicates that a device should put valid data on the data bus during a read cycle. During a write cycle this signal indicates that the MC68030 has placed valid data on the bus.
125	AS-	Output	Address Strobe indicates that a valid address is on the adress bus. The R/(W)-, FC0-FC2, and SIZ0-SIZ1 are also valid when this signal is asserted.
3,132	DSACK0 DSACK1	Input	Data Transfer and Size Acknowledge 0 and 1 indicate the completion of a requested data transfer operation and also indicate the size of the external bus port at the end of that completion.

Bus Control Signals			
Pin	**Signal**	**Type**	**Description**
131	STERM-	Input	Synchronous Termination indicates that the addressed port size is 32-bits and that the data is to be latched on the next falling clock edge for a read cycle. This active lowsignal is tied high in the FALCON030 System.
Cache Control Signals			
Pin	**Signal**	**Type**	**Description**
122	CIIN-	Input	Cache Inhibit Input prevents data from being loaded into the MC68030 instruction and data caches. This signal is ignored during all write cycles.
Interrupt Control Signals			
Pin	**Signal**	**Type**	**Description**
70,69,68	IPL0- IPL1- IPL2-	Input	Interrupt Priority Level 0-2 provide an indication of an interrupt condition and the encoding of the interrupt level from a peripheral or external prioritizing logic. IPL2- is the most significant bit of the level number.
7	AVEC-	Input	Autovector indicates that the MC68030 should generate an automatic vector during an interrupt acknowledge cycle.
Bus Control Signals			
Pin	**Signal**	**Type**	**Description**
20	BR-	Input	Bus Request indicates that an external device needs to become the bus master.
16	BG-	Output	Bus Grant indicates that the MC68030 will release ownership of the bus when the current processor bus cycle completes.
17	BGACK-	Input	Bus Grant Acknowledge indicates that an external device has become bus master.
Bus Exception Control Signals			
Pin	**Signal**	**Type**	**Description**
84	RESET-	I/O	Reset is used to initiate a system reset. As an input the MC68030 is reset. As an output only external devices are reset.
129	HALT-	Input	Halt indicates that the processor should suspend bus activity or, when used with BERR, that the processor should retry the current cycle.
130	BERR-	Input	Bus Error indicates that an invalid bus operation is being attempted or, when used with HALT-, that the processor should retry the current bus cycle.

Other Signals			
Pin	Signal	Type	Description
6	CLK	Input	Clock is the input clock to the MC68030. In the FALCON030 system it can be selected through the COMBO IC to be either 16 MHz or 8 MHz.
65,71,73	EM0 EM1 EM2	Input	Emulator support signals. These signals are tied high.
L6, K4, K10,H3, H11,F2, F11,D4, D10,C6	Vcc	Input	Power supply for MC68030
L5, L7 - L9,J3,J11, G3,G11, F3,F11,E 3,E11,C5, C7,C9	GND	Input	Ground for MC68030.

2.1.2 Optional MC68882 Coprocessor

The FALCON030 system comes equipped with a socket for an optional Motorola MC68881/MC68882 coprocessor. The coprocessor interfaces to the MC68030 via standard MC68000 bus transfers and is clocked at the same rate as the MC68030. Both data transfers and exception processing are done at the request of the coprocessor, allowing memory management, address errors, bus errors, and bus arbitration to function as if the instructions were being executed by the MC68030.

2.1.2.1 MC68882 Pin List and Signal Description

Pin	Signal	Type	Description
26-22	A0-A4	Input	Address Bus signals are used by the MC68030 to select the CIR locations in the CPU address space. Both A0 and SIZE- signals are tied high in the FALCON030 system to indicate a 32-bit data bus.
1,2,3,64-68,62,60-33	D0-D31	I/O	Data Bus signals D0-D31 serve as the general-purpose data path between the MC68030 and MC68882.

Pin	Signal	Type	Description
18	SIZE-	Input	Size is used in conjunction with the A0 signal to configure the MC68882 for 32-bit operation. SIZE- is tied high in the FALCON030 system for 32-bit data bus operation.
21	AS-	Input	Address Strobe indicates a valid address on the address bus and valid signals for chip select (CS-) and Read/Write (R/(W)-).
29	CS-	Input	Chip Select enables the MC68030 to access the MC68882's CIRs.
28	R/(W)-	Input	Read Write indicates the direction of a bus transaction. A high indicates a read from the MC68882, a low indicates a write to the MC68882.
20	DS-	Input	Data Strobe indicates that valid data is on the data bus during a write bus cycle.
31-32	DSACK0- DSACK1-	Output	Data Transfer Size and Acknowledge 0 and 1 indicate the completion of a bus cycle to the MC68030. The MC68882 asserts both signals upon the assertion of CS-.
13	RESET-	Input	Reset causes a reset of the MC68882.
11	CLK	Input	Clock is the input clock of the MC68882 and is the same frequency as the input clock of the MC68030.
4	SENSE-	I/O	Sense is tied high in the FALCON030 system to indicate the MC68882 is present.
10,16,17, 27,43,52-53, 61	Vcc	Input	Power for the MC68882.
5,6,7,8,9, 12,14,19, 30,41,51, 63	GND	Input	Ground for the MC68882.

2.1.3 ROM

One socket is provided in the system for the installation of ROM (read only memory) IC. The total amount of ROM shipped with the system is 512Kbytes. The ROM is accessed through a 16-bit bus path via the DATA0-DATA15 lines.

By default the system supports 125ns ROMs. An image of the first eight bytes of ROM resides in the first eight bytes of the system RAM area. The first eight bytes, located at 0x00000000-0x00000007, are accessible only in supervisor mode.

Any attempt to write or attempt to read from this in user mode causes a bus error. The full ROM memory map resides at addresses 0x00E00000-0x00EFFFFF.

The tasks performed by the system ROM are as follows:

- System Initialization
- Boot from Floppy or Hard disk
- TOS Operating System

2.1.4 System RAM

System RAM is physically made up of a daughter card containing 8 256K X 4, 8 1M X 4, or 32 4M X 1 DRAMs located in two banks. This architecture yields configurations of 1 Mbyte, 4 Mbytes, or 16 Mbytes of RAM used in a dual-purpose role for both system memory and video memory.

The daughter board is plugged into the main logic card via a 30-pin and 50-pin dual connector. This implementation also provides a full 32-bit data path to the VIDEL IC via the D0-D31 data bus lines. The standard configuration shipped with the system is 1Mbyte. Even though a total of 16 Mbytes of RAM may be available with 4M X 1 DRAMs installed, for compatibility with the STE, only 14 Mbytes of RAM may be accessed.

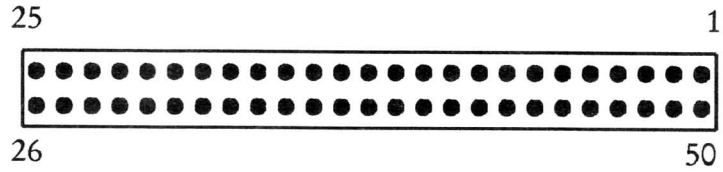
The RAM is addressed via eleven address lines (A0-A10). Row and Column selection is accomplished through the XRAS0, XRAS1, XCAS0L, XCAS0H, XCAS1L, and XCAS1H signals. Write enable for the RAM is provided by the XWE signal. On-board accesses to RAM are usually four clock cycles long, with no parity or ECC correction. Video data is accessed using fast page mode in bursts of 17 32-bit words. The data will fill the video FIFO in the VIDEL IC. The Memory Daughter Board identifies the amount of RAM present via two pins used on the Memory Daughter Board 50-pin connector.

The first 800 bytes, 0-0x800, are accessible only in supervisor mode. Any attempt to read or write to these locations in user mode causes a bus error.

2.1.5 COMBO IC

2.1.4.1 System RAM Connector Pin List

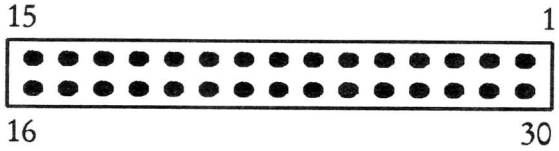
2.1.4.1.1 50-in Connector J17



50-Pin Connector J17

Pin	Signal	Pin	Signal
1	Ground	2	Vcc
3	Memory Data 15	4	Memory Data 14
5	Memory Data 13	6	Memory Data 12
7	Memory Data 11	8	Memory Data 10
9	Ground	10	Vcc
11	Memory Data 9	12	Memory Data 8
13	Memory Data 7	14	Memory Data 6
15	Memory Data 5	16	Ground
17	Vcc	18	Memory Data 4
19	Memory Data 3	20	Memory Data 2
21	Memory Data 1	22	Memory Data 0
23	Memory Size 0	24	Ground
25	Vcc	26	Ground
27	Vcc	28	Memory Data 16
29	Memory Data 17	30	Memory Data 18
31	Memory Data 19	32	Memory Data 20
33	Memory Data 21	34	Ground
35	Vcc	36	Memory Data 22
37	Memory Data 23	38	Memory Data 24
39	Memory Data 25	40	Memory Data 26
41	Ground	42	Vcc
43	Memory Data 27	44	Memory Data 28
45	Memory Data 29	46	Memory Data 30
47	Memory Data 31	48	Memory Size 1
49	Ground	50	Vcc

2.1.4.1.2 30-Pin Connector J6



30-Pin Connector J6

Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	Ground	4	Memory Address 8
5	Memory Address 7	6	Memory Address 6
7	Memory Address 5	8	Memory Address 4
9	Memory Address 3	10	Memory Address 2
11	Memory Address 1	12	Memory Address 0
13	Ground	14	Vcc
15	Vcc	16	Ground
17	Ground	18	Vcc
19	Memory Address 10	20	Memory Address 9
21	Write Enable	22	Row Address Select 0
23	Row Address Select 1	24	Column Address Select 0 High
25	Column Address Select 0 Low	26	Column Address Select 1 High
27	Column Address Select 1 Low	28	Ground
29	Vcc	30	Vcc

2.1.5 COMBO IC

The COMBO IC contained in the FALCON030 system integrates several functions. These can be summarized as follows:

- Memory Control Unit (MCU)
- Interrupt Priority and Illegal Condition Detection
- Clock Dividers
- Chip Selects
- Paddle Circuitry
- Joystick Circuitry
- Light Gun Circuitry
- Blitter (Graphics Coprocessor)

2.1.5.1 Memory Control Unit (MCU)

The Memory Controller portion of the COMBO IC takes addresses from the address bus (A1-A23) and converts them to Row and Column Addresses for DRAM with RAS and CAS Strobes. It also generates chip selects for ROM and I/O peripherals. All RAM accesses are controlled by the MCU, which is programmable for up to 14 Megabytes of memory.

Memory size is determined via two configuration pins set in hardware on the Memory Daughter Board. The Memory Controller refreshes the dynamic RAMs and loads the VIDEL IC with display data. The Memory Controller produces all of the addresses for video, refresh, and CPU/DMA on the multiplexed address bus.

2.1.5.2 Interrupt Mask and Status Control

The COMBO IC in the FALCON030 system is used both for the masking of interrupts and the storing of current interrupt status. The interrupt priorities in the system are as follows:

Interrupt Level	Priority
7 (Highest)	Open (Bus)
6	MFP Interrupts and DSP
5	85C30 LAN IC
4	Vertical Blanking (VSYNC)
3	Open (Bus)
2	Horizontal Blanking (HSYNC)
1 (Lowest)	Open (Bus)

Hardware within the COMBO IC allows the enabling of interrupt levels 1 and 3 as external VPA positive edge interrupts. This allows the use of either interrupt level for devices such as the parallel port or IDE port. Hardware is also present allowing the use of interrupt level 5 as a external negative edge interrupt. The COMBO IC uses the output signals IPL0-IPL2 to tell the microprocessor the priority of the interrupt being requested.

2.1.5.2.1 Interrupt Priority Level Signal Definition

IPL2	IPL1	IPL0	Interrupt Level
1	1	0	Level 1
1	0	1	Level 2
1	0	0	Level 3
0	1	1	Level 4
0	1	0	Level 5
0	0	1	Level 6
0	0	0	Level 7

2.1.5.3 Bus Error Circuitry and Illegal Condition Detect

Bus error circuitry is contained in the COMBO IC that causes a bus error signal (BERR) to be sent to the 68030 if certain conditions occur. These conditions are listed as follows:

- A bus cycle is not concluded within 16 micro seconds (programmable to 32usec)
- An attempt to write to ROM
- Writing the wrong size data into a register
- Writing system memory when in user mode

2.1.5.4 Clock Dividers

The COMBO IC takes the 32-MHz clock and outputs 16 MHz, 8 MHz, 4 MHz, and 500-kHz clocks.

2.1.5.5 Chip Selects

The COMBO IC decodes addresses to generate chip selects to the 6850s (N6850), MFP (MFPSC), VIDEL Video Chip (VCS), Real-Time Clock (RTCCS), Programmable Sound Generator (SNDCS), Coprocessor (FPUCS), Memory Controller, Cartridge ROM (ROM3, ROM4), IDE Hard Disk (HIDECS0, HIDECS1), and Operating System ROM (ROM2).

2.1.5.6 Paddle Circuitry

The COMBO IC contains the circuitry necessary to interface a pair of paddles through the joystick port. Input signals PAD0X, PAD1X, PAD0Y, and PAD1Y are used for direction control feed from the paddles themselves. The PADRST signal is used as a paddle reset.

2.1.5.7 Joystick Circuitry

The COMBO IC also contains the circuitry necessary to support the interface of a pair of joysticks to the system. Input signals JOYRH and JOYRL are read enables, while JOYWH and JOTWL are write enables. The BUTTON signal is used as a fire button enable signal.

2.1.5.8 BLITTER

The BLITTER contained inside the COMBO IC is a graphics coprocessor designed to handle the extra burden of graphics video generation on the microprocessor. This section performs bit aligned block transfers required in graphics generation, which adds to the capabilities of the microprocessor. The BLITTER section also contains a barrel shifter.

2.1.5.9 Light Gun Circuitry

The light gun causes a pulse on the XPEN signal which is used in the COMBO IC to latch the current values of the horizontal and vertical counters. This value can then be read by the microprocessor to determine the raster position of the light gun.

2.1.5.10 COMBO IC Pin List and Signal Description

Pin	Signal	Type	Description
1	BMODE	Input	The BMODE pin is used to indicate to the COMBEL IC whether the current bus master is a 68030 or 68000 type device. When a 68030 type device is the bus master the BMODE pin will be pulled low. The BMODE pin is normally pulled high, indicating 68000 type bus masters.
95,90,82, 68,65,63, 29,24,17, 15,12,7, 188,185, 178,177, 170,162, 143,135, 128,126, 121	A1-A23	I/O	This 23 bit bus is used for address. For MCU it is used only as an input address bus. For Blitter it is used as input address bus when it is a bus slave or as output address bus when it is a bus master.
122,127, 134,142, 176,169, 184,187, 11,15,23, 25,64,69, 91,94	D0-D15	I/O	This 16 bit bus is used for data.
186	AS-	I/O	Address strobe indicates that there is a valid address on the address bus. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.
171	UDS-	I/O	Upper data strobe controls the flow of data on the data bus together with LDS- and R/(W)-. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.

Pin	Signal	Type	Description
179	LDS-	I/O	Lower data strobe controls the flow of data on the data bus together with UDS- and R/(W)-. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.
129	R/(W)-	I/O	Read/Write defines the data transfer as read when high or write when low. It also controls the flow of data on the data bus together with LDS- and UDS-. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.
119	DTACK-	Output	Data transfer acknowledge indicates to the CPU or the current bus master that the data transfer is complete.
116	BR-	Output	Bus Request is an open drain output used to request control on the system bus. Other bus masters can also pull this line low to request control on the system bus.
124	BGI-	Input	Bus Grant is the bus grant input from the CPU in response to bus request.
198	BGACK-	Output	Bus grant acknowledge is sent to the CPU in response to the bus grant. While the Blitter is the bus master BGACK is active.
173,172, 166	IPL0- IPL1- IPL2-	Output	Interrupt priority outputs to the CPU. The COMBO encodes these lines with the proper interrupt priority code.
42	BERR-	Output	Bus Error indicates to the CPU that the current bus cycle did not terminated in the required timeout, or an address that is not in the correct I/O space was issued. Any other bus master can also pull this line low to indicate a bus error situation.
190	VPA-	Output	Valid peripheral address is output to the CPU and used to control the ACIA devices.
6	VMA-	Input	Valid memory address input from CPU. Used to control the ACIA devices.
141,133,1 23	FC0 FC1 FC2	I/O	Function codes are inputs for MCU. They are inputs for Blitter when it is a bus slave. They are outputs from Blitter when it is a bus master.
20	CLK	Input	Clock is a 32Mhz internal clock from FALCON030 motherboard.
150	TOK	Input	Keyboard transmit OK holds a transmitted character to keyboard until TOK turns HI.
139	TXD	Input	Input to COMBO of data transmitted to keyboard.

Pin	Signal	Type	Description
151	MFPINT-	Input	MFP interrupt input.
202,175, 174,72	EINT1 EINT3 EINT5 EINT7	Input	External interrupt inputs.
112	BINT-	Output	Not Connected.
19	EVEN_ODD	Input	Even/odd frame input from video shifter. 1=ODD, 0=EVEN.
138,125, 73,	PAD0X- PAD1X- PAD0Y- PAD1Y-	Input	Paddle active low inputs.
191	CPUCLK	Output	16Mhz output clock to CPU and other I/O's.
193,192	CLK4 CLK8	Output	4Mhz and 8Mhz output clocks.
163	KHZ500	Output	500Khz output clock.
197	MFPCS-	Output	MFP chip select.
199	ROM2-	Output	Socketed ROM chip select.
200,201	ROM3- ROM4-	Output	Cartridge ROM chip select.
8	SNDCS	Output	Chip select for PSG.
9	SNDIR	Output	Direction control for PSG chip.
71	VCS	Output	Video chip select.
30	VLD	Output	Active output to strobe DRAM data into shifter INPUT BUFFER.
33	HINT-	Input	Horizontal interrupt from video chip.
34	VINT-	Input	Vertical interrupt from video chip.
60	VREQ	Input	Video request signal.
31	IACK-	Output	Interrupt acknowledge to CPU.
32	N6850	Output	ACIA 6850 chip select.
44	RDAT-	Output	Read DRAM control line to video chip.
45	WDAT-	Output	Write DRAM control line to video chip.
136	PADRST-	Output	Paddle reset.
137	BUTTON-	Output	Fire buttons read enable.
147,148	JOYRH- JOYRL-	Output	Joysticks read enable lines.
140,146	JOYWE- JOYWL-	Output	Joysticks write enable lines.
36	IDEIOW-	Output	IDE I/O Write signal.
35	IDEIOR-	Output	IDE I/O Read signal.
37,38	IDECS0 IDECS1	Output	IDE chip select.
59	RESET-	Input	Reset input from CPU.

Pin	Signal	Type	Description
43	R8006-	Output	Control line to enable reading I/O address FF8006.
113	FPUCS-	Output	FPU Chip Select.
120,114, 97,96,84, 77,61,39, 10,189, 149	MAD0-10	Output	DRAM address bus.
46	WE-	Output	DRAM write enable.
18,21	RAS0- RAS1-	Output	DRAM row address select lines.
22,62	CAS0H- CAS1H-	Output	DRAM CAS HIGH select lines.
70,83	CAS0L- CAS1L-	Output	DRAM CAS LOW select lines.
74	RAMH	Output	Address select control to the VIDEO SHIFTER to select the low or high DRAM word in 16 bit video bus. 0 - select the low word.
75	RTCCS-	Output	Real-time clock chip select.
76	RTCAS-	Output	Real-time clock address strobe.
85	RTCDS-	Output	Real-time clock data strobe.
89	SCCAB	Output	SCC Channel select.
165	SCCRD-	Output	SCC read signal.
164	SCCWR-	Output	SCC write signal.
88	SCCIACK-	Output	SCC interrupt acknowledge.
87	SCCWAIT-	Input	Active low input pin to support SCC.
115	BGO	Output	BGO used for arbitration daisy chaining.
86	TEST	Input	Test pin.
163	KHZ500W	Output	Switched 500 KHz clock used for controlling 6850 that transmits keyboard data.
96	POR	Input	Power on reset.
99	TEST2	Input	Test 2 pin.
	VDD	Input	Five power lines. Connected to 5V.
	GND	Input	Five ground lines.

2.1.6 DMA Support

The FALCON030 system contains a DMA controller which provides three channels of DMA for the computer. The ACSI DMA channel from the ST product line is fully contained and has been modified slightly to accommodate a 5380 SCSI controller as well as the AJAX FDC. A record and playback DMA channel for digital sound data are also contained in this chip. The playback channel is compatible with the existing eight bit stereo and mono modes from the STE and TT products and has sixteen bit stereo added. For audio DMA to take place, the memory controller inside the SDMA IC is programmed with the starting and ending address of the RAM buffer.

The DMA controller is set up to select the source and the number of 512 byte blocks to transfer, and then the FDC or external peripheral is given the command to send or receive data. The entire block of data is then transferred to or from memory without intervention by the CPU. The FDC or peripheral generally asserts its interrupt line to signal the completion of the transfer (and the availability of status information).

2.1.6.1 DMA Pin and Signal List

Pin	Signal	Type	Description
138,139, 140	FC0-FC2	I/O	68030 bus function code. These lines are normally inputs. They become outputs during DMA when the 68030 bus is granted. Only values of 5 and 6 (supervisor program and data) will allow I/O access. A value of 5 is output during DMA.
30,28,27, 26,25,24, 22,21,20, 18,17,15, 14,13,12, 11,10,8,7, 6,5,4,3	A1-A23	I/O	68030 bus address. These lines are normally inputs. They become outputs during DMA when the 68030 bus is granted. They are used to select registers during I/O and to address memory during DMA.
136,135, 134,132, 131,130, 129,128, 126,124, 123,122, 121,119, 118,117	D0-D15	I/O	68030 bus data. These lines are inputs for I/O writes and DMA reads and outputs for I/O reads and DMA writes. They are used for data transfer between the chip and the 68030 bus.
36	AS-	I/O	68030 bus address strobe. This line is an input during I/O and an output during DMA. It is used to qualify the value on the address bus.
35	LDS-	I/O	68030 bus lower data strobe. This line is an input during I/O and an output during DMA. It is used to qualify the data on data lines D0-D7.
34	UDS-	I/O	68030 bus upper data strobe. This line is an input during I/O and an output during DMA. It is used to qualify the data on data line D8-D15.
33	R/W	I/O	68030 bus read write. This line is an input during I/O and indicates a read of the chip when high and a write to the chip when low. This line is an output during DMA and indicates a read of the bus when high and a write to the bus when low.

Pin	Signal	Type	Description
38	DTACK-	I/O	68030 bus data acknowledge. This line is an output during I/O and indicates to the 68030 bus master that the current cycle can be terminated. During DMA this line is input to determine when to terminate a DMA cycle.
39	BERR-	Input	This signal is used to terminate a DMA cycle when the system detects a bus error. It is provided to prevent system lockup when a bus error occurs during DMA.
40	BR-	Output	This output is driven low when the 68030 bus is needed to perform DMA cycles.
41	BGI-	Input	A low on this input indicates that the 68030 bus is granted and that the chip can assume control of the bus at the completion of the current cycle, if one is in progress, or immediately.
43	BGO-	Output	This output is provided to support a daisy chain on the bus grant line to arbitrate multiple bus requests. When the chip is not requesting the bus, this output is driven to match the BGI- input else it is driven high (inactive).
44	BGA-	I/O	This output is driven low when the chip assumes the bus after the request grant handshake. When DMA operations have been completed and the chip releases the bus, this line is driven high then tri-stated.
45	RESET-	Input	A low on this input resets the chip and clears any current operational mode.
76	UWD	Output	This output is the data signal of the three wire MicroWire bus.
75	UWC	Output	This output is the clock signal of the three wire MicroWire bus.
74	UWEN-	Output	This output is the enable signal of the three wire MicroWire bus.
58	SMCLK	Input	This input is the master timing clock for the sound DMA channel.
32	BMODE	Input	This input is driven by the Bus Master. It is low for 68030 Bus Masters and high for 68000 Bus Masters.
70	PLYDATA	Output	Serial sound data to DSP Connector.
71	PLYCLK	Output	Clock signal for PLYDATA. It is controlled by the receive matrix.
69	PLYSYNC	I/O	This signal is an output when in continuous clock mode, and an input when in gated clock mode.

Pin	Signal	Type	Description
67	RECDATA	Input	This is the sound data supplied by an external device connected to the DSP. This signal can be fed to one of four devices. DMA In, DSP RX, Conn RX, or Internal DAC.
68	RECCLK	Output	This is the clock signal for RECDATA.
65	RECSYNC	I/O	This signal is an output when in continuous clock mode, and an input when in gated clock mode.
59	SCLOCK	Output	This is the master clock signal for the CODEC. It has two sources. The internal 25.175MHz for 50kHz samples, and the EXT_CLOCK supplied on the DSP connector.
62	ASCLK	Output	This is the serial clock for ASDIN and ASDOUT.
61	ASSYNC	Output	This is the bit and frame sync information for the CODEC. Its format is a two-bit wide pulse every 32-bits. The two-bit wide pulse occurs every 256 ASCLKs.
63	PSGN	Input	This is the serial data from the CODEC. It is sampled on the falling edge of ASCLK.
64	ASDOUT	Output	This is the serial data for the DAC. ASDOUT changes on the falling edge of ASCLK.
2	SINT	Output	This output is low when sound DMA is active and high otherwise. It will make a high to low transition at the beginning of a frame of sound data and a low to high transition at the end of the frame. This signal can be programmed to come from either the record or play channels.
142	SCNT	Output	This output is similar to SINT but is wider.
72	TEST	Input	When this input is high, the ACSI sector count can be read in the high byte of the ACSI status register. Also a low to high transition on this signal increments the sound DMA address counters and the ACSI sector prescale and count. This pin should be tied low for normal system operation.
141	DSKIRQ-	Output	FDINT high or HDINT- low make this output low.
77	FDINT	Input	This input affects DSKIRQ- only.
78	HDINT-	Input	This input affects DSKIRQ- only.
79	FRQ	Input	Active high DMA request from the FDC.
80	FCS-	Output	Active low chip select to the FDC.
83	HRQ	Input	Active high DMA request from the SCSI controller.
84	HCS-	Output	Active low chip select to the SCSI controller.

Pin	Signal	Type	Description
84	HCS-	Output	Active low chip select to the SCSI controller.
82	ACK-	Output	Active low DMA acknowledge to the SCSI controller.
86,87,88, 89,91,92, 93,94	CD0-CD7	I/O	Data bus for the FDC and SCSI controller.
98,97,96	CA0-CA2	Output	Register address to the and SCSI controller. Used to select FDC or SCSI controller registers during I/O.
100	CRW	Output	A high means transfer from the FDC or SCSI controller. A low means transfer to the FDC or SCSI controller.
99	CRW-	Output	The inverse of CRW.
101	DISKCHNG	Input	Status input for the floppy density select register.
102,103	MODE1 MODE2	Output	Status outputs for the floppy density select register.
114,115	MDET1 MDET2	Input	Status inputs for the floppy density select register.
104	CLK32I	Input	Feedback for the 32 Mhz oscillator.
105	CLK32O	Output	32 Mhz oscillator output.
106	CLK8	Output	Free running 32 Mhz clock divided by four.
113	CLK2	Output	Free running 32 Mhz clock divided by 16.
112	FCCLK	Output	32 Mhz clock divided by 1, 2, or 4 as selected by the floppy density select register.

2.1.7 Real-Time Clock

The FALCON030 system includes a Real-time Clock chip. When the system is powered on the real-time clock is powered by the main PCB power supply. In the event of a power failure, or when the system is powered off, the real-time clock is powered by a 3.6v lithium battery.

This allows the date, time, and configuration data to be maintained even when there is no power to the unit. 50 bytes of battery backed-up RAM is also provided for storing diagnostic and configuration data.

The real-time clock provides time of day (down to one second resolution) and date. The RTC contains an integrated battery and crystal. The chip is accessed through two consecutive word ports. The first word is a write-only port used to set the real-time clock chip address desired. The second word is the read-write data port.

When doing a write to a clock chip register, a double word write can be performed. The first word would set the address, and the second word would load the data.

2.1.7.1 Real-Time Clock Pin and Signal List

Pin	Signal	Type	Description
1	MOT	Input	This signal is tied high to select Motorola bus timing.
4-11	AD0-7	I/O	These are the multiplexed address data pins for the Real-Time Clock.
13	CS-	Input	This signal is used to select the Real-Time Clock.
14	AS	Input	This signal is used to latch addresses into the Real-Time Clock.
15	R/(W)-	Input	This signal is used to select data flow direction to the static RAM. A high selects a read operation. A low selects a write operation.
17	DS-	Input	This signal is used to latch data to or from the static RAM.
18	RESET-	Input	This signal is used to reset the RTC.
19	IRQ-	Output	This signal is used to send an interrupt to the system.
23	SQW	Output	This pin is not connected in the FALCON030 system.
24	Vcc	Input	+5V Power to RTC.
12	GND	Input	Ground for RTC.
16,20,21, 22,23	N/C	——	No Connect.

2.1.8 System Timing and Bus Control

There are six system resources that use the system memory separate from the microprocessor. In order of highest to lowest priority these are:

- Expansion Bus (optional using CPU/BGO)
- Video
- DMA
- Refresh
- Blitter (Graphics coprocessor inside COMBO IC)
- Expansion Bus (using daisy-chained BG)

Only two of these arbitrate for the system bus in a normal manner. These are the DMA and Blitter. The DMA chip which resides in the FALCON030 system contains the bus arbitration logic which arbitrates for either DMA disk transfers or DMA sound accesses. DMA arbitration has a higher priority than does the Blitter.

Video accesses in the system are done in Page Mode. Any video request for memory access will interrupt other DRAM access cycles, whether they are microprocessor, DMA, or Blitter, by inserting wait states into the current bus cycle. This is accomplished by holding off the DTACK signal. While the current cycle is in wait states, the memory bus is used for the video access. When the video cycle terminates, the DTACK signal is asserted and the current cycle is allowed to complete. Refresh cycles operate in the same manner.

2.1.8.1 68000 Bus Decode PAL U68

PAL U68 is used to generate Bus Grant for 68000 type devices. It also generates the BMODE signal used to inform the SDMA and COMBO IC that a 68000 type device is accessing the bus. 68000 type devices typically require an extra clock cycle, as opposed to 68030 devices, to complete strobe and handshaking signals. The DSP data strobe signal is also generated by this PAL.

2.1.8.2 68000 Bus Decode PAL U63

PAL U63 is used to generate the Expansion Data, Bus Error, and Data Transfer Acknowledge signals to the system. It also generates the Data Transfer Size and Acknowledge 1 signal.

2.1.8.3 68000 Bus Decode PAL U62

PAL U62 is used to generate 68000 compatible Upper and Lower Data Strobes (UDS, LDS), Valid Memory Address (VMA), Read/Write (RW), and Size 1 (SIZ1) bit.

2.1.8.4 68000 Bus Decode PAL U67

PAL U67 decodes the address for the DSP (56001) and genrates a partial DSP decode.

2.1.8.5. 68000 Bus Decode GAL U44

GAL U44 generates DSP Chip Select, Hardware Acknowledge, Mfp Interrupt Enable Out, Interrupt Acknowledge, Mfp Interrupt, and Data Size And Transfer Acknowledge 0.

2.1.9 Configuration Switch

Two configuration switches are provided for the enabling or disabling of hardware options on the main logic board. The switches are 8-bit DIP type and are located at U56 and U57.

NOTE: It is recommended that these switches not be changed as problems could result from their improper setting.

The values of these switches is as follows:

U56

Segment	Function
1	On = 1 Wait State DRAMs OFF = 0 Wait State DRAMs
2	On = 32-bit Video Bus Off = 16-bit Video Bus
3-4	Off Off = 0 Wait State ROMs Off On = 1 Wait State ROMs On Off = 2 Wait State ROMs On On = Reserved
5-6	Not Used
7-8	Not Used

U57

Segment	Function
1-4	Not Used
5	Off = Quad Density Floppy On = Don't Care
6	Off = AJAX Installed (1.44MB) On = 1772 Installed (720K)
7	Off = No DMA Sound Hardware On = DMA Sound Hardware Installed

2.2 AUDIO/VIDEO SUBSYSTEM

2.2.1 Video System Overview

The video subsystem in FALCON030 is composed of five major components. These are as follows:

- Video RAM (Dual-purpose System and Video)
- Interrupt and Data Load Control (COMBO)
- Video Shifter (VIDEL)
- Digital to Analog Converter (DAC)
- NTSC/PAL Encoder (1377)

The FALCON030 Video Subsystem extends the existing STE video modes. Video can be generated in ST compatible modes as well as VGA, True Color, and Programmable modes. Functionality has been enhanced by the ability of the subsystem to access video memory on any even word boundary. There is an RF modulator on-board to facilitate the direct connection to TV. Video also has the capability of being GENLOCKed for sync to external video timing sources. The monitor connector supplied with the system allows for the connection of ST color and ST monochrome monitors in addition to VGA type monitors.

The video modes supported by the system are as follows:

ST Modes

Resolution	Bit Planes	Colors	Palette Colors
320 X 200	4	16	4096/262,144
640 X 200	2	8	4096/262,144
640 X 400	1	2	4096/262,144

VGA Mode

Resolution	Bit Planes	Colors	Palette Colors
640 X 480	8	256	262,144

True Color

Resolution	Bit Planes	Colors	Palette Colors
320 X 200	15	32,768	1 Bit GENLOCK
320 X 200	16	65,536	No GENLOCK

Programmable

Resolution	Bit Planes	Colors	Palette Colors
X x Y	1,2,4,8	2,4,16,256	262,144

2.2.1.1 Video RAM

Video RAM is shared as dual-purpose memory with the rest of the FALCON030 system. The physical screen origin located at the top left corner of the screen is the start of mapped display memory.

Display memory is configured as 1, 2, 4, or 8 logical planes that are interwoven as 16-bit words into contiguous memory to form one physical plane starting at any even-word boundary.The size of this plane will depend on the video resolution and the number of colors selected. For example, 320 X 200 4 color mode would require a 32,000 byte plane.

2.2.1.2 Interrupt and Data Load Control (COMBO)

The COMBO IC is responsible for handling the interrupts generated by the VIDEL IC, and the loading of DRAM data into the video chip's input buffer. COMBO receives the interrupt signals VINT for VSYNC and HINT for HSYNC. A request for video data to be loaded into the video RAM buffer within the VIDEL IC is generated to the COMBO IC by the VREQ signal, and DRAM data is loaded into the video chip's input buffer via the VLD signal from the COMBO IC.

The starting address of display memory is placed in the COMBO IC's Video Base High, Video Base Mid, or Video Base Low Address registers by the Operating System or application. This register is loaded into the Video Address Counter (High/Mid/Low) in the COMBO IC at the beginning of each frame. The Address Counter is incremented as the Bitmap planes are read. COMBO then loads the VIDEL IC with Bitmap info 32-bits at a time.

2.2.1.3 Video Shifter (VIDEL)

The COMBO IC will load Bitmap planes into the VIDEL IC video buffer 32-bits at a time, except in XGA mode. The video shifter then loads the video shift register where one bit from each plane is shifted out and collectively used as the index to a specific STE or SP (FALCON030) palette register There are 16 word-wide color registers which comprise the STE palette and 256 double word-wide registers in the SP palette.

Each palette is programmed for 12 bits of color in STE mode, four for each red, green, and blue, or 18 bits of color in SP mode, 6 for each red, green, and blue. Therefore there are 16 x 16 x 16 or 4096 colors possible in STE mode, and 64 x 64 x 64 or 262,144 colors possible in SP mode. In monochrome mode, the color palettes are bypassed and instead provided with an inverter for inverse video controlled by bit 0 of palette register 0.

The VIDEL IC also has the ability to accept vertical sync and video clock. To inject a system clock ground pin 16 (EXT) on the monitor connector and then inject the clock into pin 15 (GENLOCK INPUT).

The internal frequency of this clock is 32.215905 MHz (NTSC) and 32.084988 MHz (PAL). VIDEL also includes the circuitry necessary to interface a light gun or pen plugged into Joystick 0. The current position that the gun or pen is pointing to is reported by these registers.

The position is accurate to within (X direction only):

- 4 Pixels in 320 x 200 Mode
- 8 Pixels in 640 x 200 Mode
- 16 Pixels in 640 x 400 Mode

Accurate to 1 pixel in the Y direction in all modes. Accuracies do not account for the quality of the light gun or pen. Note that the X position is given in pixels for 320 x 200 only. In order to get correct results in 640 x 200 mode this number needs to be shifted left one bit and in 640 x 400 modes this number needs to be shifted left two bits.

2.2.1.4 Video Digital to Analog Converter (DAC)

The Video DAC is used to take digital TTL input data from the VIDEL IC and convert it to analog RGB output. Inputs of 6-bit color info from the VIDEL are supplied to the DAC via the R2-R7, G2-G7, and B2-B7 inputs. The DAC then outputs analog R, G, and B to the monitor connector.

2.2.1.4.1 Video Digital to Analog Converter Pin and Signal List

Pin	Signal	Type	Description
40	COM	Input	Tied high in the FALCON030 system to select internal digital channel to output amplifier.
4-1,44-41	G0-7	Input	Eight bit green input data from VIDEL.
36-29	B0-7	Input	Eight bit blue input data from VIDEL.
12-5	R0-7	Input	Eight bit red input data from VIDEL.
37	RC	Input	Tied high in the FALCON030 system to select binary coding on R and B data.
25	BEXT	Input	Auxiliary blue input. Not connected in the FALCON030 system.
22	GEXT	Input	Auxiliary green input. Not connected in the FALCON030 system.
19	REXT	Input	Auxiliary red input. Not connected in the FALCON030 system.
18	ROUT	Output	Analog red output to monitor connector.
21	GOUT	Output	Analog green output to monitor connector.
24	BOUT	Output	Analog blue output to monitor connector.
38	CLK	Input	Clock input.
15,26	AVcc	Input	Chip power input.

2.2.1.5 NTSC/PAL Encoder (1377)

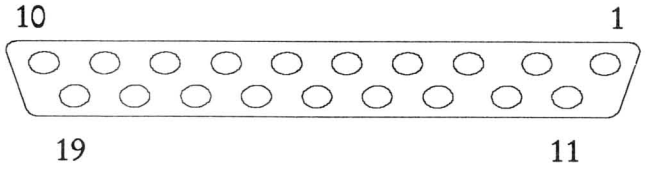
The 1377 encoder is used in the system to convert baseband RGB and sync signals into a composite TV signal.

2.2.1.6 VIDEL Pin and Signal List

Pin	Signal	Type	Description
60,59,57, 55,50,39, 35,33,32, 31,29	A1-A11	Input	These are the 11 LSB of the CPU address bus.
19,20,21, 24,26,28, 34,36,37, 38,40,41, 42,43,48, 49	D0-D15	I/O	This is the CPU data bus.
78-84,87-89,92-85	MD0-31	I/O	This is the 32 bit DRAM data bus. Data is read from this bus when the DRAM is read. Data is written onto this bus when the DRAM is written.
18,17,13, 2,11,9,51, 52,53,54, 56,58,64-68,72	R0-R5 B0-B5 G0-G5	Output	These are the 3x6 digital RGB outputs.
10	DOTCK	Output	This is the clock for the DAC.
8	MONO	Output	This is the monochrome output when not in XGA. In CONTROL XGA mode it is the pixel control.
96	COLOR	Output	This is a timing signal for composite video generation for NTSC TV.
62	CSYNC	Output	This signal is the composite sync output.
47	VREQ	Output	This is the video request active high output.
44	CLK32	Input	This is a 32 Mhz clock input. Used in non VGA cases.
73	CLK25	Input	This is a 25 Mhz clock input for VGA cases.
14	EXTCLK	Input	This is the external Genlock clock input.
6	VSYNC-	I/O	This is the vertical sync signal. It is programmable as input or out.
114	TEST.		
3	HSYNC-	I/O	This is the horizontal sync signal. It is programmable as input or out. In case of TV it contains the full interlace support.

Pin	Signal	Type	Description
101	HINT-	Output	This is the horizontal display enable signal used for Hsync interrupt generation.
97	VINT-	Output	This is the vertical display enable signal used for Vsync interrupt generation.
7	R/(W)-	Input	This is the CPU R/W input signal. It is used to access the internal registers including CLUT. When high the registers are read to the CPU. When low the registers are written with data from the CPU.
25	VCS	Input	This is the chip select active high input. It selects the video chip for CPU read/write accesses (according to R/W) to/from the video chip internal registers or CLUT. It is controlled by the CPU DS.
66	VLD	Input	This signal informs the video chip that the data read from the DRAM is to be loaded into the video INPUT BUFFER.
22	RDAT-	Output	This active low signal enables the data read from the DRAM into the CPU data bus to enable CPU reading from the DRAM.
23	WDAT-	Output	This active low signal enables the CPU data bus into the DRAM data bus to enable CPU writing into DRAM.
70,71	CAS0- CAS1-	Output	These are the SIMMs active low CAS signals. They are ORed in the video chip and used to latch the DRAM data into the INPUT BUFFER.
2	PEN-	Input	This is the Light/gun pen input.
4	LOWP	Input	Low Power pin. Can be used to disable the clocks. It is grounded in normal applications.
5	RAMH	Input	This is an address control signal from COMBO to select the high or low DRAM word in 16 bit video bus. 0 selects low word.
85	ODD_EVEN	Output	An output pin to indicate odd/even video frames. 0 - EVEN.
86	DE	Output	Display Enable.
1	RESET	Input	Reset to VIDEL chip.
	DGND	Input	Digital ground pins.
	DVcc	Input	Digital power pins.
119	EXT	Input	Used to turn on the external Genlock logic.
112	TN	Input	Used for VLSI parametric testing.

2.2.1.7 Monitor Connector Pin List



1	Red	11	Ground
2	Green	12	Composite Sync
3	Blue	13	Horizontal Sync
4	Mono Out	14	Vertical Sync
5	Ground	15	Externa Clock Input (GENLOCK)
6	Red Return (GND)	16	EVEN_ODD
7	Green Return (GND)	17	+12 Volts for PERITEL
8	Blue Return (GND)	18	Video Master Control Bit 1
9	Audio In	19	Video Master Control Bit 2
10	Ground		

2.2.2 Audio Subsystem

The FALCON030 architecture extends the music subsystem presently available on the ST/MEGA computers. The FALCON030 mixes the output of the existing ST PSG sound system with a new DMA-driven dual-channel A-toD, D-to-A subsystem (Codec device). The FALCON030 combines these two sources for simple beeps, and can be connected to an external stereo amplifier for high-fidelity sound. In addition the resulting audio is sent to an on-board speaker which can be turned off with an general purpose bit from the PSG.

2.2.2.1 Programmable Sound Generator

The ST sound system using the General Instruments AY-3-8910/Yamaha YM-3439 Programmable Sound Generator is present in the FALCON030 system. The YM-3439 Programmable Sound Generator produces music synthesis, sound effects, and audio feedback.

With an applied clock input of 2 MHz, the PSG is capable of providing a frequency response range between 30 Hz (audible) and 124 KHz (post-audible). The generator places minimal amount of processing burden on the main system (which acts as the sequencer) and has the ability to perform using three independent voice channels. The three sound channel outputs are mixed, along with Audio In, and sent to the CODEC IC for processing. The PSG also provides the speaker gate for the internal speaker.

2.2.2.2 DMA Sound

The FALCON030 also includes a new DMA-driven sound subsystem that allows the playback or synthesis of complex waveforms at a variety of sampling rates. This feature is supported by the new Codec device which is driven from the new DMA device (same IC that controls the disk DMA cycles).

Sound in the form of digitized samples is stored in system memory. These samples are fetched from dual-purpose memory by the SDMA IC (transparent to the processor) and provided to digital-to-analog converters (DAC's) in the Codec device at a constant sample frequency specified by the user. The outputs of the DAC's are then low pass filtered into a walkman type, micro-stereo connector and to the on-board speaker.

Two channels are provided. They are intended to be used as the left and right channels of a stereo system when using the raw audio outputs from the machine. They are mixed together when fed to the on board speaker or monitor speaker. A MONO mode is provided which will feed the same data to both channels simultaneously. The only restriction placed on MONO mode is that there must be an even number of samples.

2.2.2.3 Codec IC

The Codec IC in the FALCON030 system is connected through a serial protocol to provide both an Analog to Digital (ADC) and Digital to Analog (DAC) function for in the 16-bit stereo sound system. The Codec is strapped so that the ADC operates as a conventional oversampling ADC producing stereo data at the output. The DAC operates as a conventional oversampling single bit DAC.

A serial interface is used to connect the Codec IC to the system. It is made up of a data line in, a data line out, a clock line, and a syncchronization input. Serial data from the SDMA IC to the CODEC consists of interleaved volume, control, and 16-bit stereo sound data. Volume control is achieved by changing the interleaved volume data values.

2.2.2.3.1 Codec Pin and Signal List

Pin	Signal	Type	Description
1	SSYNC	Input	The Serial Sync Input signal is used to indicate the start of a word or frame of transmissions via the serial interface.
2	RESET-	Input	The Reset input signal is used to reset the CIDC IC.
3	CLKIN	Input	The CLKIN input signal is used as the master clock of the CODEC IC. The D to A and A to D converters are driven by this input.
4	DVcc	Input	This is the power supply voltage for the CODEC IC.
5	DGND	Input	This is the ground for the CODEC IC.

Pin	Signal	Type	Description
13	PON-	Input	The Low Power Mode input signal is used to switch the CODEC to low power mode. This pin is tied to Vcc in the Falcon030.
15	ROUT	Output	The Right Analog Output pin is the right channel analog output signal.
16	LOUT	Output	The Left Analog Output pihn the left channel analog output signal.
18	POMCR	—	The Capacitor Connection pin is used for the outer feedback loop of the pulse density modulator for the right channel. It is tied to the REFBUF pin.
19	POMCL	—	The Capacitor Connection pin is used for the outer feedback loop of the pulse density modulator for the left channel. It is tied to the REFBUF pin.
20	REFBUF	—	The Buffered Internal Analog Ground pin is the buffered signal analog ground pin for the pulse density modulator capacitors.
21	REFBYP	—	The Internal Analog Ground pin is the clean analog ground pin for the analog input and output connectors.
22	REFGND	—	The Reference Analog Ground pin is the ground pin that serves as a clean ground for the CODEC IC.
23	AGND	—	The Analog Ground pin is used as an analog ground for the CODEC IC.
24	AVcc	Input	The Analog Supply Voltage pin is used to supply power to the analog circuitry of the CODEC IC.
25	RIN1	Input	The Right Analog Input Channel 1 signal is fed to this pin.
26	RIN2	Input	The Right Analog Input Channel 2 signal is fed to this pin.
27	LIN1	Input	The Left Analog Input Channel 1 signal is fed to this pin.
28	LIN2	Input	The Left Analog Input Channel 2 signal is fed to this pin.
29	MDSEL	Input	The Mode Select Input signal is used to select additional serial formats when pulled high. It is tied to ground in the Falcon030 system.
30	SBF2	Input	The Subframe Input 2 pin is used to determine what subframe the CODEC IC will be active. This pin is grounded in the Falco030 system.

Pin	Signal	Type	Description
31	SBF1	Input	The Subframe Input 1 pin is used in conjunction with the Subframe Input 2 pin to determine what subframe the CODEC IC will be active. This pin is grounded in the Falco030 system.
32	TESTEN	Input	The TestMode Enable pin is used to seitch the CODEC IC into test mode. This pin is grounded in the falcon030 system.
33-36	DI1-DI4	Input	The Digital Input 1-4 pins are used to supply digital data to the CODEC IC. These pins are grounded in the Falcon030 system.
33-40	DO1-DO4	Output	The Digital Output 1-4 pins are used to supply digital data from the CODEC IC. These pins are not connected in the Falcon030 system.
41	TEST2	Input	The Test 2 pin is used for test mode sychronization. It isnot connected in the Falcon030 system.
42	SDIN	Input	The Serial Data Input pin is used to input serial digital data to the CODEC IC.
43	SDOUT	Output	The Serial Data Output pin is used to output the analog to digital signal according to the serial interface format.
44	SCLK	Input	The Serial clock input pin is used 5to define the bit clock for theserial interface. It latches the data in on the SDIN line, and out on the SDOUT line.

2.3 I/O SUBSYSTEMS

The FALCON030 architecture supports the following device subsystems:

- IDE Hard Disk Interface.
- External SCSI II Hard Disk Port.
- Floppy disk interface sharing the ST ACSI DMA channel.
- Serial port and an external LAN port connected to SCC controller.
- A Centronics parallel printer port driven by the Yamaha YM-3439 sound chip.
- An ST/MEGA compatible intelligent keyboard, mouse, and joystick interface.
- Option for interfacing to the new Atari Universal Keyboard Controller.
- A port supporting application and diagnostic cartridges.
- Two controller ports for additional joysticks as well as light pen/gun and paddle controllers.

2.3.1 SCSI II Interface

The external hard disk drive interface is provided through a standard 5380 NCR SCSI Controller. Transfers can take place at up to 2Mbytes/second. The controller interfaces to the system through the SDMA IC.

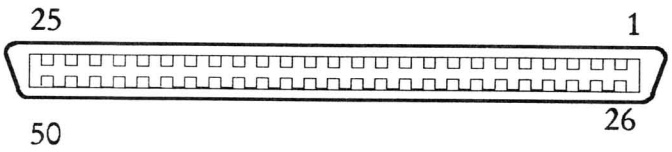
2.3.1.1 5380 SCSI Controller Pin and Signal List

Pin	Signal	Type	Description
37-41,43-44,1	DB0- to DB7-	I/O	8-bit SCSI data bus. During arbitration these lines contain the SCSI ID numbers of all devices arbitrating for the SCSI bus. During selection, these lines contain the ID number of the device which has been selected.
35	DBP-	I/O	SCSI data bus parity bit.
5	SEL-	I/O	The Select signal is asserted by the initiator to select a target. It can also be asserted by the target when reselecting it as an ititiator.
4	BSY-	I/O	Busy is asserted when the SCSI bus is active.
33	ACK-	I/O	Acknowledge is asserted by the initiator during information transfer phases in response to REQ- asserted by the target.
6	ATN-	I/O	Attention is asserted by the intiator after the successful selection of a target.
7	RST-	I/O	When active this signal indicates a SCSI bus reset condition.
32	I/O-	I/O	I/O is controlled by the target device and indicates the direction of data transfer. When low the direction of data flow is to the initator.

Pin	Signal	Type	Description
30	C/D-	I/O	Control/Data is sent by the target to indicate that control or command information is on the SCSI bus.
29	MSG-	I/O	Message is controlled by the target device and indicates a message phase of operation.
34	REQ-	I/O	The Request signal is asserted by the target device to begin the handshake needed to transfer a byte of data over the bus. The REQ- signal is negated upon the receipt of an ACK- signal by the initiator.
17	CS-	Input	Chip Select enables reading or writing from the 5380.
9	DRQ	Output	DMA Request is used to request DMA service from the DMA controller.
8	IRQ	Output	Interrupt Request is used to send an interrupt to the microprocessor.
19	IOR-	Input	The I/O Read signal is used to read the controller's registers.
13	READY-	Output	The READY signal can be used as an alternate DRQ device. This pin is not connected in the FALCON030 system.
11	DTACK-	Input	DMA Acknowledge is used to enable reading or writing of the SCSI controller's internal registers.
10	EOP-	Input	The End Of Process signal is used to indicate that a DMA transfer is to be concluded.
7	RESET-	Input	The Reset signal is used to reset the SCSI controller.
18	IOW-	Input	The I/O Write signal is used to write information to the SCSI controller's registers.
14-16	A0-2	Input	Address lines 0-2 are used to select the internal SCSI controller register which is to be accessed.
28-24,22-20	D0-7	I/O	Data lines 0-7 are the microprocessor data bus.

2.3.1.2 External SCSI Connector Pin List

The SCSI interface uses a 50 pin connector with the following pin assignment:



Pin	Signal	Pin	Signal
1-10	Ground	37	No Connect
11	+5 Volts	38	+5 Volts 1A Fuse
12-14	No Connect	39	No Connect
15-25	Ground	40	Ground
26	SCSI 0	41	ATN
27	SCSI 1	42	Ground
28	SCSI 2	43	Busy
29	SCSI 3	44	Acknowledge
30	SCSI 4	45	Reset
31	SCSI 5	46	Message
32	SCSI 6	47	Select
33	SCSI 7	48	Code/Data (C/D)
34	Parity	49	Request
35-36	Ground	50	I/O

2.3.2 Floppy Disk (FDD)

The FALCON030 floppy disk subsystem is designed around the AJAX Floppy Disk Controller supporting one floppy disk drive. It is a higher speed version of the 1772 and supports 1.44Mb (formatted) capacity drives.

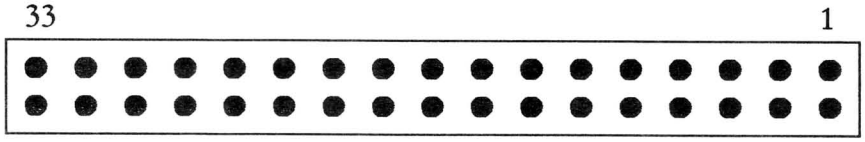
The subsystem interfaces to the dual-purpose RAM through the ACSI DMA controller, which is part of the SDMA IC. Commands and arguments are sent to the FDC by first writing to the DMA Mode Control Register to select the desired FDC register and then writing the data bytes. The standard floppy for the FALCON030 is the 3.5 inch floppy disk with the capacity of 1.44 Mbyte (formatted).

2.3.2.1 AJAX Pin and Signal List

Pin	Signal	Type	Description
1	CS-	Input	Chip Select is used to enable communications between the chip and the host interface.
2	R(W)-	Input	Read/Write- is used to control the direction of data from the internal registers in the device. A low enables a read of the registers, a high enables a write to the registers over the DAL0-7 lines.
3,4	A0,A1	Input	Address 0-1 are used to select the internal register in the device that is to be read or written.
5-12	DAL0-DAL7	I/O	The Data 0-7 lines are an 8-bit bus used to transfer data, commands, or status.
13	MR-	Input	Master Reset is used to reset the AJAX chip.
14	GND	Input	Ground for the AJAX chip.
15	Vcc	Input	Power Supply (+5V) for the AJAX chip.
16	STEP	Output	Step is used to step the read/write heads of the FDD.
17	DIRC	Output	Direction is used to select whether the FDD heads are stepped toward the center or out from the center of the FDD. A high causes the heads to step toward the center.
18	CLK	Input	Free running clock input.
19	RD-	Input	Read Data is the raw data line containing both clock and data pulses from the FDD.
20	MO	Output	Motor On is used to enable the spindle motor of the FDD.
21	WG	Output	Write Gate is used to enable writing to the FDD.
22	WD	Input	Write Data is the clock and data pulses to be written to the FDD.
23	TR00-	Input	Track 00 informs the AJAX chip that the FDD's heads are over track 0.
24	IP-	Input	Index Pulse tells the AJAX chip when the Index Hole on the Diskette has been encountered.
25	WPRT-	Input	Write Protect tells the AJAX chip that the diskette in the FDD is write protected.

Pin	Signal	Type	Description
26	DDEN-	Input	Double Density Enable is used selects FM or MFM operation of the FDD. A low is MFM.
27	DRQ	Output	Data Request is used to indicate that the internal data register is full on a read, or empty on a write.
28	INTRQ	Output	Interrupt Request is used to tell the host system that a command has been completed.

2.3.2.2 Internal Floppy Connector Pin List



Pin	Signal	Pin	Signal
1	Ground	2	Mode Select 1
3	Ground	4	Not Connected
5	Ground	6	Mode Select 2
7	Ground	8	Index Pulse
9	Ground	10	Drive Select 0
11	Ground	12	Not Connected
13	Ground	14	Not Connected
15	Ground	16	Motor On
17	Ground	18	Direction Select
19	Ground	20	Step
21	Ground	22	Write Data
23	Ground	24	Write Gate
25	Ground	26	Track 0
27	Ground	28	Write Protect
29	Media Detect 2	30	Read Data
31	Ground	32	Side Select
33	Media Detect 1	34	Disk Change

2.3.3 68901 MFP

A 68901 Multi-Function Peripheral (MFP) controller is used to provide system timers and an interrupt controller. The MFP is used in a way that is compatible with the ST.

2.3.3.1 Interrupt Control

Interrupts handled by the 68901 MFP are as follows:

- RS232 Ring Indicator Interrupt
- Sound Interrupt
- ACSI/FDD/IDE Interrupt
- MIDI Interrupt
- Keyboard/MIDI Interrupt
- DSP Interrupt
- Printer Acknowledge Interrupt
- Printer Busy Interrupt

2.3.3.2 68901 MFP Pin and Signal List

Pin	Signal	Type	Description
1	NC1	———	No Connect.
2	RXW	Input	Read/Write defines the current bus cycle as a read or write cycle. When high it is a read. When low it is a write.
3-7	RS1-5	Input	The Register Select bus bits are used to select an internal MFP register during a read or write cycle.
8	TC	Input	The Transmitter Clock input controls the serial bit rate of the transmitter within the MFP. It is tied to the Timer D output.
9	SO	Output	This is the USART serial data output line. This pin is not connected in the Falcon030 system.
10	SI	Input	This is the USART serial input data line. This pin is grounded in the Falcon030 system.
11	RC	Input	The Receiver Clock is used to control the bit rate of the receiver internal to the MFP. It is tied to the Timer D output.
12	Vcc	Input	Power to the 68901.
13	NC	———	No Connect.
14	NC	———	No Connect.

Pin	Signal	Type	Description
15	TAO	Output	Timer A Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
16	TBO	Output	Timer B Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
17	TCO	Output	Timer C Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
18	TDO	Output	Timer D Output is tied to the TC and RC pins of the 68901 to provide rate timing for transmit and receive. The serial portion of the 68901 MFP is not used in the Falcon030 system.
19	XTAL1	Input	Crystal input for timers.
20	XTAL2	Input	Crystal input for timers.
21	NC	------	No Connect.
22	TAI	Input	Timer A Input is a control signal for the Timer A internal to the MFP. It is tied to the Sound Interrupt.
23	TBI	Input	Timer B Input is a control signal for the Timer B internal to the MFP. It is tied to the Display Enable Interrupt.
24	Reset	Input	The Reset signal is used to reset the 68901.
25	IO0	I/O	General Purpose Input 0 is used as an interrupt input for Printer Busy.
26	IO1	I/O	General Purpose Input 1 is used as an interrupt input for Printer Acknowledge.
27	IO2	I/O	General Purpose Input 2 is used as an interrupt input for the MIDI.
28	IO3	I/O	General Purpose Input 3 is used as an interrupt input for the DSP.
29	IO4	I/O	General Purpose Input 4 is used as an interrupt input for Keyboard/MIDI.
30	IO5	I/O	General Purpose Input 5 is used as an interrupt input for IDE/SCSI.
31	IO6	I/O	General Purpose Input 6 is used as an interrupt input for RS232 Ring Indicator.

Pin	Signal	Type	Description
32	IO7	I/O	General Purpose Input 7 is used as an interrupt input for Sound System.
33-35	NC	———	No Connect.
36	IRQ	Output	IRQ is used to alert the 68030 that an interrupt is pending.
37	IEO	Output	Interrupt Enable Out allows any device daisy chained off the MFP to signal an interrupt if no higher priority device is requesting an interrupt.
38	IEI	Input	Tied to ground unless expansion is used. Then it is tied to the IEO pin of the expansion MFP to signal no higher priority device is requesting an interrupt.
39	CLK	Input	Input clock for the MFP.
40	GND	Input	Chip ground.
41-48	D0-D7	I/O	8-bit data bus.
49	IACK	Input	Interrupt Acknowledge from the 68030.
50	DTACK	Output	Data Transfer Acknowledge signals completion of a data transfer phase of operation.
51	DS	Input	Data Strobe is used to latch data into the MFP.
52	CS	Input	Chip Select is used to enable the MFP for access.

2.3.4 8530 Serial Communications Controller (SCC)

The Falcon030 contains an 8530 Serial Communications Controller (SCC) that provides a dual channel, multi-protocol device that provides a serial port and network LAN port. The input/output of the serial port is routed to a DB-9P connector. The input/output of the LAN port is routed to a DB-8P connector.

The PCLK input to the SCC is rated at 8 MHz. The RTXCA and RTXCB input is provided with a 3.672 MHz clock. The TRXCA input comes from the LAN connector, and the TRXCB input is rated at 2.4576 MHz.

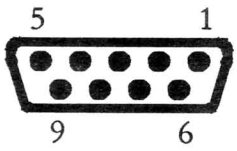
2.3.4.1 8530 Pin and Signal List

Pin	Signal	Type	Description
1-5,42-44	D0-D7	I/O	8-Bit data bus.
6	INT	Output	Interrupt Request from the SCC.
7	IEO	Output	Interrupt Enable Out is used to daisy chain several devices together. Normally it is tied to the IEI pin of the next device. It is not connected in the FALCON030 system.
8	IEI	Input	Interrupt Enable In is used to daisy chain to the next higher priority device. It is connected to +5V to indicate there is no higher priority device in the system.
9	INTACK-	Input	Interrupt Acknowledge is used to indicate that an active interrupt acknowledge cycle is taking place.
10	+5V	Input	+5 Volt power supply for the IC.
11	SCCWAIT	Output	SCC Wait Request is used to set up wait timing for CPU synchronization.
12	SYNCA	I/O	Synchronization A is used as an input or otput for channel A depending upon the mode of operation. In Asynchronous Receive Mode the pin acts as an input similar to CTS and DCD. In External Synchronization Mode this pin acts as an input and must be driven low to receive clock cycles after the last sync bit. In the Internal Synchronization Mode the pin is an output and only active during the part of the receive clock cycle in which sync characters are being received. This opin is tied to the DSRA signal.
13	RTXCA-	Input	Receive/Transmit Clock A is the clock signal for the receive/transmit circuit for channel A.
14	RXDA	Input	This is the serial data receive pin for channel A.
15	TRXCA	I/O	Transmit/Receive Clock Channel A is used to supply the transmit or reseive clock for channel A.
16	TXDA	Output	Transmit Data Channel A is used to transmit serial data on channel A.
17	P17	------	No Connect.

Pin	Signal	Type	Description
18	P18	———	No Connect.
19	DTR/REQA-	I/O	The Data Terminal Ready/Request Channel A signal is used to show the state of the DTR bit for channel A.
20	RTSA-	Output	The Request To Send Channel A signal is used to reflect the state of the Request To Send bitfor channel A.
21	CTSA-	Input	The Clear To Send Channel A reflects the state of the Clear To Send bit for channel A.
22	DCDA-	Input	The Data Carrier Detect Channel A is used to reflect the state of the DCD bit for channel A.
23	PCLK	Input	This siganl is used as the master SCC clock.
24	DCDB-	Input	The Clear To Send Channel A reflects the state of the Clear To Send bit for channel B.
25	CTSB-	Input	The Data Carrier Detect Channel A is used to reflect the state of the DCD bit for channel B.
26	RTSB-		The Request To Send Channel A signal is used to reflect the state of the Request To Send bitfor channel B.
27	DTR/REQB-		The Data Terminal Ready/Request Channel A signal is used to show the state of the DTR bit for channel B.
28	NC	———	No Connect.
29	TXDB	Output	Transmit Data Channel A is used to transmit serial data on channel B.
30	TRXCB-	I/O	Transmit/Receive Clock Channel A is used to supply the transmit or reseive clock for channel B.
31	RXDB	Input	This is the serial data receive pin for channel B.
32	RTXCB-	Input	Receive/Transmit Clock A is the clock signal for the receive/transmit circuit for channel B.

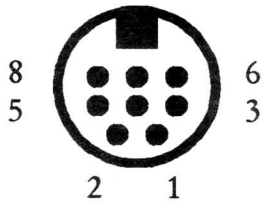
Pin	Signal	Type	Description
33	SYNCB-	I/O	Synchronization A is used as an input or otput for channel A depending upon the mode of operation. In Asynchronous Receive Mode the pin acts as an input similar to CTS and DCD. In External Synchronization Mode this pin acts as an input and must be driven low to receive clock cycles after the last sync bit. In the Internal Synchronization Mode the pin is an output and only active during the part of the receive clock cycle in which sync characters are being received. This opin is tied to the DSRB signal.
34	W/REQB-	------	No Connect.
35	GND	Input	Ground.
36	NC	------	No Connect.
37	D/C-	Input	Data/Control Select is used to select the type of information being transferred by the SCC. A high = data.
38	CE-	Input	This is the chip enable signal for the SCC.
39	A/B-	Input	This is the chaneel select input for the SCC.
40	WR-	Input	This signal is used to indicate a write operation.
41	RD	Input	This signal is used to indicate a read operation.

2.3.4.2 8530 Serial Port Pin and Signal List



Pin	Function
1	Carrier Detect (In)
2	Receive Data (In)
3	Transmit Data (Out)
4	Data Terminal Ready (Out)
5	Ground
6	Data Set Ready (In)
7	Request to Send (Out)
8	Clear to Send (In)
9	No Connect

2.3.4.3 SCC LAN Connector Pinout



Pin	Function
1	Output Handshake
2	Input Handshake
3	Transmit Data-
4	Ground
5	Receive Data-
6	Transmit Data+
7	(Reserved)
8	Receive Data+

2.3.5 Parallel Printer Port

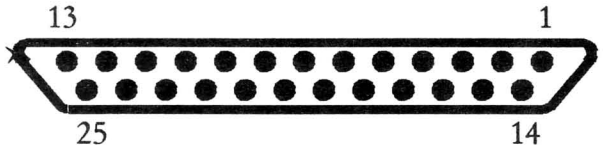
The FALCON030 architecture includes a bi-directional 8-bit parallel printer port that implements a subset of the Centronics standard.

This interface is through the General Instruments AY-3-8910 or Yamaha YM-3439 Programmable Sound Generator (PSG) chip. It is pinned out in a DB25S. The Centronics STROBE signal is generated from a PSG bit.

The Centronics BUSY and Printer Acknowledge signals from the printer connects to one of the parallel input lines of the MFP to permit interrupt driven printing. Eight bits of read/write data are handled through I/O port B on the PSG at a typical data transfer rate exceeding 4000 bytes/second.

2.3.5.1 Parallel Port Connector Pin List

The parallel port uses a DB 25 pin S connector with the following pin assignments:



Pin	Function	Pin	Function
1	Centronics Strobe	2	Data 0
3	Data 1	4	Data 2
5	Data 3	6	Data 4
7	Data 5	8	Data 6
9	Data 7	10	Acknowledge
11	Centronics Busy	12	Not Connected
13	Not Connected	14	Not Connected
15	Not Connected	16	Not Connected
17	Select In	18	Ground
19	Ground	20	Ground
21	Ground	22	Ground
23	Ground	24	Ground
25	Ground		

2.3.6 Keyboard Interface

The keyboard interface is completely compatible with the ST/MEGA computers. The keyboard is equipped with a combination mouse/joystick port and a joystick only port. The keyboard transmits encoded make/break key scan codes (with two key rollover), mouse/trackball data, joystick data, and time-of-day.

The keyboard receives commands and sends data via bidirectional communication implemented with a MC6850 Asynchronous Communications Interface Adapter (ACIA). All keyboard functions, such as key scanning, mouse tracking, command parsing, etc. are performed by a HD6301V1 8-bit microcomputer unit. (See the Atari, Intelligent Keyboard (ikbd) Protocol, February 26, 1985.)

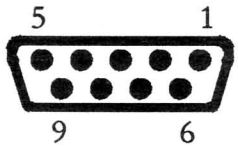
FALCON030 also has hooks to interface to the new Atari Universal Keyboard Controller. These hooks prevent data overrun both to and from the keyboard controller.

2.3.7 Mouse and Joystick Interface

The Atari two-button mouse is a mechanical, optomechanical, or optical mouse with the following minimal performance characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second, and maximum pulse phase error of 50%. The joystick is a four direction switch-type joystick with one fire button.

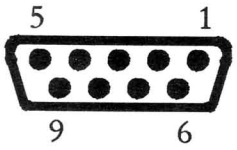
2.3.7.1 Mouse and Joystick Interface Connector Pin List

Mouse/joystick0 uses a DB9 pin P connector with the following pin assignment:



Pin	Function
1	Xb Pulse/ Up Switch
2	Xa Pulse/ Down Switch
3	Ya Pulse/ Left Switch
4	Yb Pulse/ Right Switch
5	Not Connected
6	Left Button/ Fire Button
7	Power
8	Ground
9	Right Button/ Joy1 Fire

Joystick1 uses a DB 9 pin P connector with the following pin assignment:



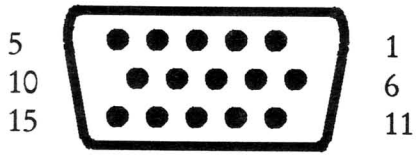
Pin	Function
1	Up Switch
2	Down Switch
3	Left Switch
4	Right Switch
5	Reserved
6	Fire Button
7	Power
8	Ground
9	Not Connected

2.3.8 Game Controller Ports

The FALCON030 system includes two STE compatible game controller ports which can be used for paddles, joysticks, or a light pen. These ports are enabled by the COMBO IC and interface directly to the data bus of the 68030.

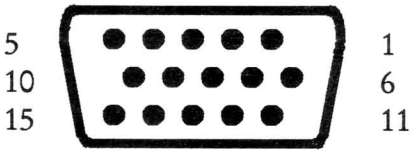
2.3.8.1 Game Controller Pinout

Controller A



Pin	Function	Pin	Function
1	Up 0	2	Dn 0
3	LT 0	4	RT 0
5	Pad 0Y	6	Fire 0/Light Gun Pulse
7	+5 VDC	8	Not Connected
9	Ground	10	Fire 1
11	Up 1	12	Dn 1
13	LT 1	14	RT 1
15	Pad 0X		

Controller B



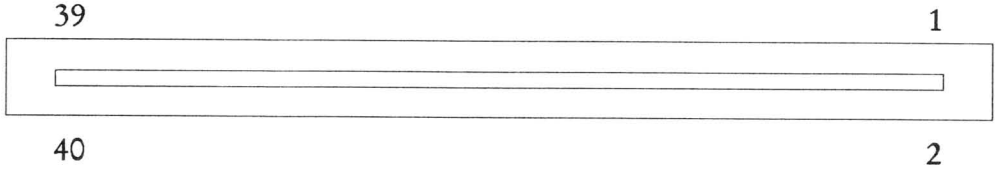
Pin	Function	Pin	Function
1	Up 2	2	Dn 2
3	LT 2	4	RT 2
5	Pad 1X	6	Fire 2
7	+5 VDC	8	Not Connected
9	Ground	10	Fire 3
11	Up 3	12	Dn 3
13	LT 3	14	RT 3
15	Pad 1Y		

2.3.9 ROM Cartridge

The FALCON030 cartridge port is fully compatible with ST cartridge. The cartridge is physically connected through a 40 pin card edge connector ROM cartridge slot. Cartridge ROMs are mapped to a 128K memory region starting at 0x00FA0000, extending to 0x00FBFFFF.

2.3.9.1 ROM Cartridge Connector Pin List

If not in a plastic housing, the cartridge must be installed with the chips facing down. The cartridge uses a 40 pin card edge S connector with the following pin assignment:



Pin	Function	Pin	Function
1	+5VDC	2	Power +5Vdc
3	Data 14	4	Data 15
5	Data 12	6	Data 13
7	Data 10	8	Data 11
9	Data 8	10	Data 9
11	Data 6	12	Data 7
13	Data 4	14	Data 5
15	Data 2	16	Data 3
17	Data 0	18	Data 1
19	Address 13	20	Address 15
21	Address 8	22	Address 14
23	Address 7	24	Address 9
25	Address 6	26	Address 10
27	Address 5	28	Address 12
29	Address 11	30	Address 4
31	ROM3 Select	32	Address 3
33	ROM4 Select	34	Address 2
35	Upper Data Strobe	36	Address 1
37	Lower Data Strobe	38-40	Ground

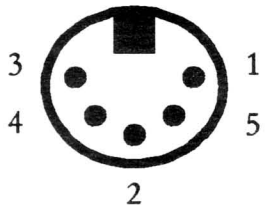
2.3.10 Musical Instrument Digital Interface (MIDI)

The MIDI allows the integration of the FALCON030 series with music synthesizers, sequencers, drum boxes, and other devices possessing MIDI interfaces. High speed (31.25 Kbaud) serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (the MIDI OUT also includes MIDI THRU data).

The MIDI communicates through the MC6850 Asynchronous Communications Interface Adapter (ACIA) to the system bus. The data transfer rate is a constant 31.25 Kbaud of 8-bit asynchronous data.

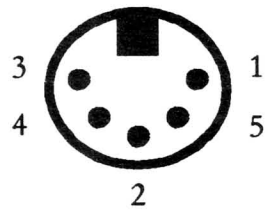
2.3.10.1 MIDI Connector Pin List

The MIDI OUT/THRU uses a circular DIN 5 pin S connector with the following pin assignment:



Pin	Function
1	Thru Transmit Data
2	Shield Ground
3	Thru Loop Return
4	Out Transmit Data
5	Out Loop Return

The MIDI IN uses a circular DIN 5 pin S connector with the following pin assignment:



Pin	Function
1	Not Connected
2	Not Connected
3	Not Connected
4	In Receive Data
5	In Loop Return

2.3.11 Digital Processor Interface (DSP)

The FALCON030 system includes a Digital Signal Processor (DSP) which can be used for complex audio and video processing. The DSP is located across the data and address buses of the 68030, and also has access to 32K of 24-bit, zero wait-state static RAM. The RAM can be used for information storage. Some of the various uses for the DSP would be sound and music synthesis, special sound effects, and 3D graphics modeling.

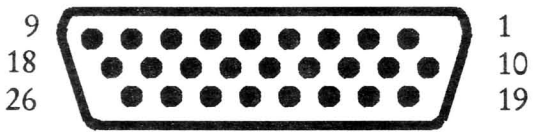
2.3.11.1 DSP Pin and Signal List

Pin	Signal	Type	Description
53,54,57, 58,60,61, 65,67,68, 70,71,75, 76,77,79, 80	A0-A15	Output	16-bit Address bus.
81,82,85, 86,87,88, 92,93,94, 96,97,99, 102,104, 105,106, 108,109, 113,114, 115,118, 119,120	D0-D23	I/O	24-bit data bus.
52	PS-	Output	Program Memory Select is driven when external program memory is referenced. This pin is not connected in the FALCON030 system.
49	DS-	Output	Data Memory Select is driven when external memory is referenced.
48	X/(Y)-	Output	This signal is used to select which external memory space is referenced by the DS- signal. This pin is not connected in the FALCON030 system.
47	RD-	Output	Read Enable is asserted to read the external memory on the data bus (D0-D23).
46	WR-	Output	Write Enable is asserted to write the external memory on the data bus (D0-D23).

Pin	Signal	Type	Description
45	BR-	Input	Bus Request allows another device to become master of the external address and data buses (D0-D23, A0-A15). This pin is tied high in the FALCON030 system.
43	BG-	Output	This signal is used to acknowledge an external bus request. It is tied high in the FALCON030 system.
123	MODA/ IRQA-	Input	Mode Select A is a dual function pin used to select the initial operating mode of the DSP56001 and to receive interrupts from and external source. This pin is tied high in the FALCON030 system selecting Mode A.
121	MODB/IRQ B-	Input	Mode Select B is a dual function pin used to select the initial operating mode of the DSP56001 and to receive interrupts from and external source. This pin is tied to reset in the FALCON030 system.
124	RESET-	Input	Reset is used to reset the DSP56001.
25,22,20, 19,16,15, 14,11	HD0-7	I/O	The Host Data Bus is used to transfer data between the host system and the DSP56001.
5,2,1	HA0-2	Input	The Host Address Bits are used to select the Host Interface Registers.
9	HR/(W)-	Input	This signal selects the direction of Host processor access.
8	HEN-	Input	This signal is used to enable the transfer of data on the host data bus.
10	HREQ-	Output	This signal is used to request service from the host processor.
6	HACK-	Input	This signal is used to receive acknowledge of a request made for DMA transfers or for interrupt acknowledge from the host processor.
27	RXD	Input	Not Connected in the FALCON030 system.
28	TXD	Output	Not connected in the FALCON030 system.
29	SCLK	I/O	Not connected in the FALCON030 system.
31,40,37	SC0-2	I/O	These pins are used for control by the Synchronous Serial Interface.
32	SCK	I/O	Serial bit rate clock for the Synchronous Serial Interface.
42	SRD	Input	Data is input into the SSI Receive Shift Register on this pin.

Pin	Signal	Type	Description
39	STD	Output	Data is transmitted from the SSI Transmit Shift Register on this pin.
	Vcc	Input	Power supply for DSP56001.
	GND	Input	Ground for DSP56001.
127	EXTAL	Input	External 32 MHz clock input.

2.3.11.2 DSP Connector Pin List

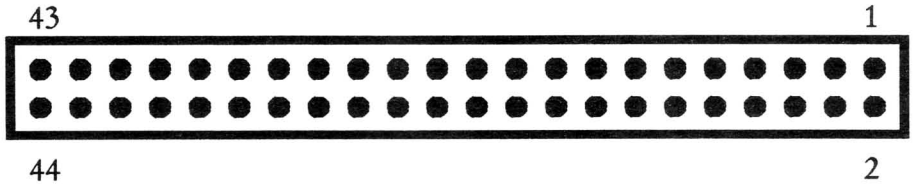


Pin	Function	Pin	Function
1	GP0	2	GP2
3	GP1	4	SDMA Play Data
5	SDMA Play Clock	6	SDMA Play Synchronization
7	No Connect	8	+12V
9	+12V	10	Ground
11	SYNC Serial I/F Control 0	12	SYNC Serial I/F Control 1
13	SYNC Serial I/F Control 2	14	Ground
15	Synchronous Serial Data In	16	Ground
17	+12V	18	Ground
19	SDMA Record Data	20	SDMA Record Clock
21	SDMA Record Synchronization	22	DSP Interrupt
23	SYNC Serial I/F Data Out	24	SYNC Serial I/F Clock
25	Ground	26	External Clock (GENLOCK)

2.3.12 IDE Interface

The FALCON030 is equipped with an IDE interface. IDE drives can be connected through an internal 44-pin connector. Chip selects and direction control for the IDE interface are provided by the COMBEL IC. The interface resides across the data bus using data bits 0-16. Four address bits are used to control the IDE interface (A2-A4).

2.3.12.1 IDE Connector Pin List



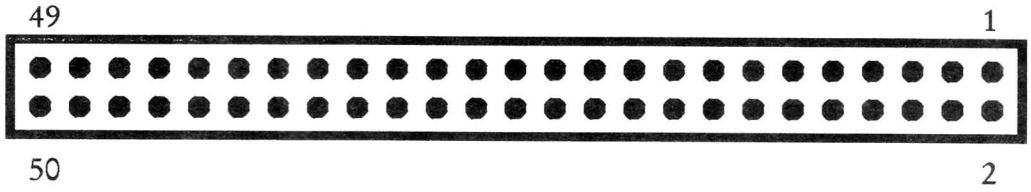
Pin	Function	Pin	Function
1	RESET	2	Ground
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DADA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	Ground	20	KEY
21	N/C	22	Ground
23	IOW	24	Ground
25	IOR	26	Ground
27	N/C	28	N/C
29	N/C	30	Ground
31	IRD	32	N/C
33	ADDR 3	34	N/C
35	ADDR 2	36	ADDR 4
37	CS0	38	CS1
39	ACT	40	Ground
41	VCC	42	VCC
43	Ground	44	N/C

2.3.13 Expansion Connector

The FALCON030 contains an expanxion port connector for use with expansion boards designed for the system. The expansion port is made up of one 50-pin connector and one 30-pin connector. The connectors interface to the system through the data and address bus. External interrupts numbers 1 and 3 are provided to the connector. External bus masters can also be plugged into the expansion connector, and signals are provided for bus control and synchronization.

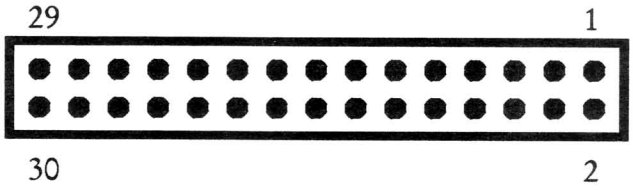
2.3.13.1 Expansion Connector Pin List

50-pin Connector J19



Pin	Function	Pin	Function
1	Ground	2	Ground
3	Bus Grant Acknowledge	4	Address Strobe
5	Lower Data Strobe	6	Upper Data Strobe
7	Read/Write	8	Data Transmit Ack
9	Function Code 2	10	Function Code 1
11	Function Code 0	12	BMODE
13	No Connect	14	Interrupt Ack
15	Combel Bus Grant Acknowledge	16	Bus Request
17	Reset	18	Halt
19	Bus Error	20	IPL0
21	IPL1	22	IPL2
23	Clock	24	Vcc
25	Vcc	26	Address 23
27	Address 22	28	Address 21
29	Address 20	30	Address 19
31	Address 18	32	Address 17
33	Address 16	34	Address 15
35	Address 14	36	Address 13
37	Address 12	38	Address 11
39	Address 10	40	Address 9
41	Address 8	42	Address 7
43	Address 6	44	Address 5
45	Address 4	46	Address 3
47	Address 2	48	Address 1
49	Expand	50	No Connect

30-pin Connector J20



Pin	Function	Pin	Function
1	Data 14	2	Data 13
3	Data 12	4	Data 11
5	Data 10	6	Data 9
7	Data 8	8	Data 7
9	Data 6	10	Data 5
11	Data 4	12	Data 3
13	Data 2	14	Data 1
15	Data 0	16	Data 15
17	Ground	18	Ground
19	Ground	20	Expansion Bus Grant
21	Interrupt 1	22	External CPU Bus Grant
23	500 kHz Clock	24	No Connect
25	MFP Interrupt Enable In	26	MFP Interrupt
27	Interrupt 3	28	Vcc
29	Vcc	30	Vcc

2.4 SYSTEM STARTUP

After a RESET (power-up or reset button) the 68030 will start executing at the address pointed to by locations 4-7, which is ROM (the MCU within the COMBO IC maps the first 8 bytes of ROM at E00000 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM. The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse). (RESET.)
2. Read the longword at cartridge address FA0000. If the data read is a magic number, execute from the cartridge (cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations are valid). If not, initialize the memory controller.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if successful.
12. If no boot disk, load the desktop ROM on board ROM.

2.5 SYSTEM ERRORS

The 68030 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen. The number of bombs equals the number of exceptions which occurred.

System errors may or may not be recoverable. Errors in loading files from disk may cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

2.5.1 Number of Bombs and Meaning

2: BUS ERROR. COMBO IC asserted bus error.

3: ADDRESS ERROR. Processor attempted to access word or long word sized data on an odd address.

4: ILLEGAL INSTRUCTION. Processor fetched an instruction from ROM or RAM which was not a legal instruction.

5: ZERO DIVIDE. Processor was asked to perform a division by zero.

6: CHK INSTRUCTION. This is a legal instruction, if software uses this, it must install a handler.

7: TRAPV INSTRUCTION. See Chk instruction.

8: PRIVILEGE VIOLATION. CPU was in user mode, tried to execute a 68030 instruction that can only be performed in supervisor mode.

9: TRACE. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.

10: LINE 1010 EMULATOR. CPU read an instruction which has '1010' as its most significant nibble. Used by TOS for low level graphics software routines.

11: LINE 1111 EMULATOR. CPU read an instruction which has '1111' as its most significant nibble.

12: Unassigned, should be no occurrence.

13: Coprocessor Protocol Violation. A read of the coprocessor has resulted in an illegal value.

14: Format Error. The format word passed to the coprocessor was invalid.

15: Uninitialized Interrupt. An interrupt was received that had not been reset.

16-23: Unassigned, should be no occurance.

24: SPURIOUS INTERRUPT. Bus error during interrupt processing.

25-31: AUTOVECTOR INTERRUPT. Numbers 4 and 2 are used, others should have no occurrence.

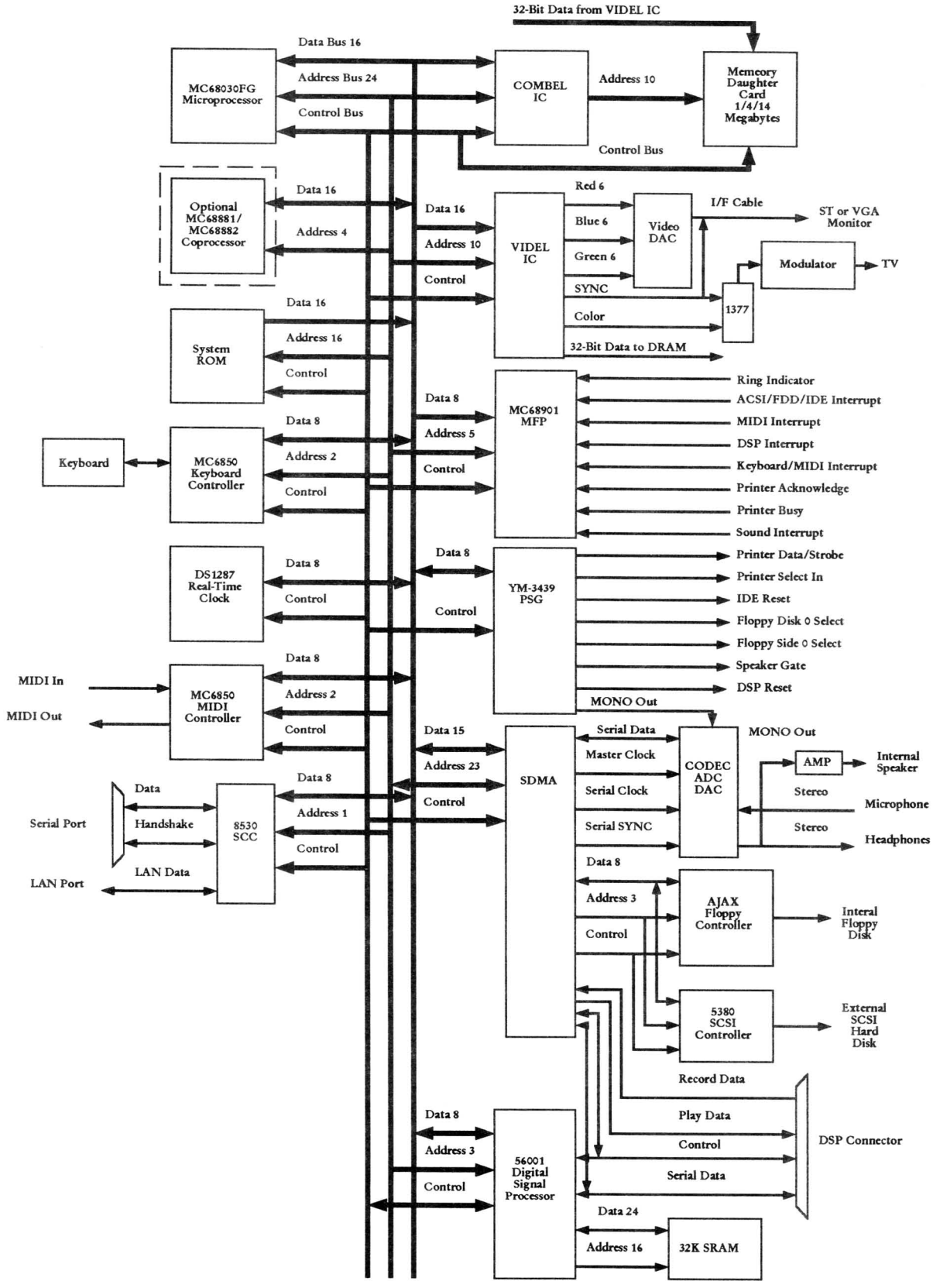
32-63: TRAP INSTRUCTION. CPU read instruction which is used to generate a software exception (such as the entry to GEMDOS, VDI, or AES).

64-79: MFP interrupts.

80-127: Reserved for Atari use.

128-255: Unused.

2.6 Overall Block Diagram



SECTION THREE
TESTING

3.0 OVERVIEW

The FALCON30 diagnostic cartridge is the latest in a series of test diagnostics designed for testing the ST, STE, and MEGA STE Atari line of computers. Although specific to the new FALCON30 computer it's functions, operation, and menu set up were designed for ease of transition for prior users of Atari diagnostic cartridges as well as accommodating new operators with it's "user friendly" features.

As in previous versions of Atari diagnostics they are menu driven and are selectable in sequence, number of cycles, and particular test/tests executed. By "shopping" in the menu the user can create a unique test set for a particular test environment or use the canned sequences designed for manufacturing, field service, or as part of a customer acceptance test.

The diagnostics are seperated into several different categories, with a menu screen for each one. Initially a menu will be displayed requiring a choice between manufacturing type tests and field diagnostics. The tests and menus descripbed in this section are for the field diagnostics menu. The production test sequences are not covered beyond their initial disply in the opening menu.

The field disgnostic menu is divided into three groups or tests. The "unattended" tests are designed for minimal operator interaction. They are go/no go tests that indicate success with a green screen, a single audio tone, and a pass message. Failures are indicated with a red screen, multiple tones (in a different pitch) and a failure message.

The next group require an operator to determine success or failure based on observations or interactions with the diagnostics. Some of the tests in this category include the audio and video tests.

The final group are a set of tools or utilities that can be used for reading/writing memory, changing clock speeds, setting up the real time clock etc.

On power up and before the main menu is displayed a short self test is automatically performed. If the machine fails this test the red screen/multiple audio tones/failure message is presented.

NOTE: The diagnostics will always attempt to echo to and look for input from the standard RS-232 port. In case of screen or keyboard failure, an external terminal can be connected to this port and a limited set of the diagnostics executed.

If power up is normal then the main menu will be displayed on the monitor.

Since the FALCON30 system is quite complex, it should not be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68030 processor may be helpful.

Economics will be an important consideration; due to the low cost of the FALCON30 computer line, little time can be justified in troubleshooting down to the component level when it may be cheaper to replace the functional sub-assembly.

3.1 TEST EQUIPMENT

The following equipment is required for a complete exercise of the diagnostic cartridge on the FALCON30 computer:

- FALCON30 Diagnostic Cartridge
- Blank Double Sided 3 1/2-inch Diskette
- Blank High Density 3 1/2-inch Diskette
- IDE Hard Disk Drive
- SCSI External Hard Disk Drive
- Atari SC1224 RGB Monitor (or similar)
- Atari SM124 Monochrome Monitor (or similar)
- VGA Monitor
- RS232 Loop-Back Connector
- MIDI Loop-Back Cable
- LAN Loop-Back Connector
- Printer Port Test Cable
- Mouse Port Test Cables (2)
- Game Port Test Cables (2)
- Monitor Test Cable
- Monitor Adaptor Connectors
- ST DMA Test Fixture
- STE Test Fixture
- Expansion Test Fixture
- Audio Loopback cables (2)
- DSP Loopback connector
- Dual Channel oscilloscope

3.2 TEST CONFIGURATION

With the power switch off, install the Diagnostic Cartridge with the label facing UP.

Important: if the cartridge does not have the plastic enclosure; **BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN.**

Connect cables from the STE test fixture into the parallel port and joystick/mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug the Audio Loopback cables into the MIC and Headphovne jacks. Plug the DSP Loopback Connector into the DSP Connector. Plug the LAN Loopback Connector into the LAN Port. Plug the color monitor into the monitor output (a monochrome monitor can be used instead).

Make sure the switch on the STE test fixture is in the position marked INT, otherwise the program will not proceed past the initialization.

Power on the unit. Some tests will be run automatically, in a few seconds the menu screen should appear. If the screen appears, skip down to Section 3.4: FALCON30 Diagnostic Cartridge, below. If not read the next Section 3.3: Troubleshooting a Dead Unit.

If the unit is being used as a terminal for a host computer, it should be disconnected from the host before using the diagnostic; otherwise, the host may think someone is logged on, and will send messages which will act like keystrokes input to the diagnostic.

3.3 TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered on and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the power supply for proper voltages to verify the unit is powered on and making sure the monitor is working.

1. Connect a terminal to the RS232 port of the unit under test (U.U.T.). You can use an STE running the VT52 terminal emulator program – see the owner's manual for setting up the VT52. The cable should connect pin 2 (serial out) of the U.U.T. to pin 3 (serial in) of the terminal and vice versa. Connect pin 5 (ground) to pin 7. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity (this is the default condition for the VT52 emulator).

   Insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to troubleshoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to Section 3.4: FALCON30 Diagnostic Cartridge for information on using the cartridge.

   If no activity is seen on the RS232 port or display, continue with (2) below.

2. Disassemble the computer so that the printed circuit board is exposed (see section 4. Disassembly). Power up the computer. Using an oscilloscope, verify the 32 MHz clock to the COMBO IC. If it is not present, replace the oscillator. Check the 16 MHz clock to the 68030 CPU. If it is not present replace the COMBO IC. Then check the HALT pin of the 68030 CPU. It should be TTL high. If so, go on to 3 below. If not, the CPU is halted. The reasons may be: (a) bad reset circuit, (b) double bus error. (c) bad CPU.

   A. Check for a bad Reset circuit by observing signal on input of the the HALT line.

   B. Check for a double bus error by observing BERR input of the CPU as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and COMBO is genrating the error. Verify the clocks to COMBO, tracing back to the oscillator (master clock) if necessary.

      If still failing, the CPU is unable to read ROM, enable the display, select the 68901 for RS232 operations, or the 68030 is defective. Check the XROM3 and XROM4 chip select inputs to the Cartridge ROM. If they are not present, replace the COMBO IC. Check the display enable output of the VIDEL IC. If not present check the input clocks and Vcc connections to the VIDEL IC and replace the VIDEL IC or the failing components. If there is still no RS232 display, check the MFP chip select signal.

If CS is present, check the Data Strobe (DS) signal to the MFP. If it is also present, check the DTACK signal. If DS and CS, along with RS1-RS5 and D0-D7 are active and DTACK is not being asserted, the MFP could be bad. Replace the MFP IC.

C. There is no way to check for a bad CPU other than by elimination of the other possibilities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

3. If the CPU is not halted, it should be reading instructions from the ROM (cartridge, if installed) and data and address lines will be toggling (if not, replace CPU). At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 8) while powering on the unit with the cartridge installed. If the data is being sent, trace it through the 1488 driver. Note that -12V is required for RS232. If all looks good, there may be something wrong with the connection to the terminal.

   Verify also the output of the VIDEL IC. If using an RGB monitor, check the outputs to the summing resistors for R, G, and B. Note that if DE is not going high, no picture will be output. If using monochrome, check the MONO output pin. Also check the input to the VIDEL IC, pin 8, MONO. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the VIDEL IC instead of MONO.

   If the VIDEL IC is outputting a signal, but the picture is unreadable, there is probably a problem with the screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

3.4 FALCON30 DIAGNOSTIC CARTRIDGE

The FALCON30 Diagnostic Cartridge is used to detect and isolate component failures in FALCON30 computers. This section gives a brief guide to its use with a description of each test, error codes or pass/fail criteria, and recommendations on repair.

3.5 POWER UP SEQUENCE

The diagnostic program performs system initialization and testing on power-up. As devices and sub-systems are initialized and/or tested check messages will be displayed on the monitor. On normal power-up these messages will be cleared before the main menu is displayed and a single audio tone is sounded. This first display contains status information as well as a test selection menu.

If the machine fails before the menu is displayed, the last check message on the monitor points to the trouble area. If a recoverable failure occurs the screen will turn red (dark background in monochrome) with a message indicating the failure. In addition several rapid audio tones (different in pitch from the "PASS" tone) will be sounded. Before the main menu is displayed the user must press the space bar to clear the error message/messages.

The lowest 2 Kbytes of RAM is tested on power-up. If a location fails, the error will be printed to the RS-232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or RAM for system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red).

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS-232 port. The diagnostic program will look for keystrokes from the RS-232 device. If the display is unreadable, again the RS-232 terminal should be used. All messages will always be echoed to the RS-232 port as well as displayed on the screen.

3.5.1 Initialization And Check Sequence

3.5.1.1 RAM

Memory will be sized and saved for display later in the main menu. Pointers to data written, data read, and address location shall be incremented in registers in the CPU and, on error, dumped out the standard RS232 port for possibly display. The system RAM will be tested as follows:

3.5.1.1.1 All Ones - All Zeros (I1)

All ones are placed on the lower 16 bits of the data lines (at address 8), verified, rewritten with all zeros, and verified again. This is to ensure that at least the lower 16 data lines are not in a stuck condition and testing can continue.

3.5.1.1.2 Walking Ones - Walking Zeros (I1)

First a one bit is rotated through a field of zeros and verified. Then a zero bit is rotated through a field of ones and verified. This is again done at address eight and is a quick check for shorted data lines.

3.5.1.1.3 Address Line Shorting (I2)

The first 2K of RAM (8 - 7ff) is cleared. Then RAM from 800 to the top of sized memory is filled with ones. The low 2K of RAM is then checked for disturbance.

3.5.1.1.4 Low 2K RAM Address Check (I3)

Each word address location from 8 to 800 is loaded with its least significant 8 bit address and verified. Then the complement 8 bit address is written and verified. This is a check for correct locations being addressed.

3.5.1.1.5 RAM Stack Test

This test will cycle back to the beginning of initialization until a safe stack area is found or stopped by the user. Errors will be dumped out to the display as well the standard RS232 port showing data written, data read, and address location.

3.5.1.2 System Initialization

If working RAM is found then 68030 exception handlers are loaded, MFP set up, interrupts enabled, video and RS232 display set up, etc. Finally screen memory will be cleared and the first ok message "Hello world" displayed.

3.5.1.3 Check Messages

At this point the system is functioning enough that check messages should be readable on either the monitor or over the RS232 port. As each sub-system test routine is entered a check/start message will be displayed. As each routine is completed an exit message will be sent indicating status. Every effort will be made to recover from a check but if a non-recoverable error occurs the last check message will indicate the testing location.

3.5.1.3.1 Bus Error Check

A bus error is forced by writing to ROM. A check is then made to verify that bus error occurred. If a bus error did not occur the screen will turn red and a message sent to the displays. (RS232 and monitor). If the bus error worked then only a status message is sent.

3.5.1.3.2 FPU Check

A check is made to see if a co-processor is in the system. Status is sent to the monitors and saved for later recall by menu selection. "No FPU" is not considered an error so the screen will not be forced red.

3.5.1.3.3 FALCON30 Specific Checks

Do checks and report/save status.

3.5.1.3.4 PSG And Printer Port Initialization:

PSG is initialized, printer port set up to make test fixture outputs high impedance and sound is shut off.

3.5.1.3.5 Timer Testing - Genlock

The timing test is called. (see timing test module in the main menu). This module generates it's own enter and status messages. It tests the MFP timers and reports status to the calling routine. If an error is sent then no further clock tests can be executed and timer testing is over. If the MFP is ok then it's timers will be used as a reference for testing the main system clock/clocks as well as verification of an external "Genlock" clock.

The usual enter message is generated. A MFP timer is started and the CPU is placed in a tight instruction loop. If the MFP times out before the CPU quits it's instruction loop, then the system clock is too slow or an external clock from the Genlock test board is now the system clock. In either case the display will be disabled and a continuous tone generated until the system is reset.

If the MFP has not timed out then the system clock is ok. The usual status message is sent and the test ends.

As part of the Genlock test, the pixel control bit in the SP shift mode register is set. The operator will use a scope to verify that the Genlock key pin on the test board (STE test PCB) is toggling at a video pixel rate. This part of the test should be done during the XGA video test and not while operating under control of the external Genlock clock on the STE test board.

3.5.1.4 Clean Up

The keyboard is initialized, the clock speed is set, and cache is turned off. After a one second delay, the screen is cleared of messages and then the main menu is called.

3.5.2 Error Message Summary

3.5.2.1 Initialization Errors

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM sizing error. Uppermost address fails.
I6 Bus Error handling failed. Bus Error occurred (on purpose), but caused a crash (e.g. system was unable to read the vector from RAM).
I7 Bus Error not detected. COMBEL not asserting Bus Error or the signal is not reaching the 68030.
T0 MFP timers failed.
T1 Vertical sync timing failed.
T2 Horizontal sync timing failed.
T3 Display Enable Interrupt failed.
T4 Memory Controller video address counter failed.
T5 PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.
T6 Floppy Disk Controller Bus test. AJAX chip is causing a bus error by staying on the data bus too long.
K0 Stuck key
K1 Keyboard controller is not responding.
K2 Keyboard controller reports error.

3.5.2.2 Check Message Summary

- Entering bus error check
- Exit bus error check
- Entering FPU check
- Exit FPU check
- Entering (FALCON30 spec.) check/checks
- Exit FALCON30
- Init PSG/ printer port
- Entering Timer test
- Testing MFP, Glue timing, Video
- Return from Timer test
- Init. kybd, set clocks, disable cache
- Jump to main menu

3.6 TEST MENU

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. Normally the menu will be divided into three main areas; Unattended tests, Operator tests, and Diagnostic Tests. If the Real-Time Clock battery has failed since the unit left the factory the menu may appear with less selections in the Unattended and Operator sections. These sections are provided for factory test of the unit only. Do not select any of the tests contained in those sections. Select only D for Diagnostic Tests Menu.

FALCON30 Production Test Rev. X.X
(c) 1992, Atari Corp.

X Mbytes RAM — Keyboard revision 2 60 Hz
O.S. Version X — USA NTSC

UNATTENDED

P Pre Burn-In
B Burn-In
F Post Burn-In
I In Process Assembly
U Assembled Unit

OPERATOR

A Audio
V Video
K Keyboard
H IDE Hard Disk

==========

D Diagnostic Tests Menu
E Error Report

Enter Letter:

3.6.1 Diagnostic Tests Menu (Typical)

Menu displayed on the diagnostic screen

FALCON30 Field Service Diagnostic Test Rev. X.X
(c) 1992, Atari Corp.

X Mbytes RAM — Keyboard revision 2 60 Hz
O.S. Version X — USA NTSC

UNATTENDED

R RAM & SRAM	O O.S. ROMS	M MIDI
S SCC Serial	T Timing	D DSP Port
F Floppy Disk	P Printer/Joy/Game	L Real Time CLK
G Short BLiT	I SCSI Port	X Expansion Bus

Q Run all unattended tests (R,O,M,S,T,D,F,P,L,G,I,X)
Z Run unattended internal tests (R,O,T,F,L,G)

OPERATOR

A Audio V Video K Keyboard H IDE Hard Disk

E Examine/Modify system
? Help

Enter letter(s) and RETURN:

3.6.2 MAIN MENU TEST SELECTION

3.6.2.1 Unattended Tests

A single test or any combination of tests will be selected by typing the corresponding letter or letters, then typing the RETURN key. To run repeated cycles of a test or (tests), the last letter typed is followed with the number of cycles to run.

For example, "RSM25", will run RAM, Serial, and MIDI tests 25 times. If 0 is entered, testing will be continuous. The ESC key will quit a test cycle. In most cases control will be returned to the keyboard immediately.

An RS232 terminal may be used for input and display. Note, the Serial RS232 test will not pass if this terminal is installed in place of the loopback test plug.

If an error occurs, an error message will be displayed and the screen will turn red. When the test completes, Pass or Fail will be displayed, and the screen will turn green or red (red = dark background in monochrome).

If multiple tests are run and an error occurs on any test, the screen will remain red, even if successive tests pass. Once the test has halted, the SPACE BAR is used to return to the menu.

The last selections in the unattended tests are canned group tests executed with a single letter and a C/R. If an individual or custom sequence is not required selecting one of the canned versions will automate the testing procedure.

3.6.2.1.1 (R) RAM & SRAM TEST

The RAM and SRAM test starts by testing the 32K SRAM hooked up to the DSP. Several patterns are written and checked including all ones, all zeros, all AA, all 55, a random write pattern, and a walking ones patters. Next the system RAM is tested. System RAM is tested in three stages: low 2 kbytes, middle (up to 64k), and from 64k to top. The test patterns used are: all 1s, all 0s, a counting pattern (data=low word of the address), reverse counting pattern (data=complement of address low word). The counting pattern is copied from the top and bottom of a 32 Kbyte buffer into the current 32 Kbytes of video RAM, then shifts video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64k boundaries is checked by writing a unique pattern in the last 256 bytes of each 64k block. The DSP SRAM is also tested in this procedure.

If an error occurs, the screen will turn red accompanied by several beep tones. The error code is displayed, followed by the address, data written, data read, and the bits which did not agree. E.g.: " R2 45603E W:603E R:613C bad bits: 1,8".

RAM & SRAM Error Codes

R0	Low memory failed while setting up to run test.
R1	Failed walking 1s or 0s.
R2	Failed address (counting pattern).
R3	Failed 64k boundary test. Probable failure in Memory Controller.
R4	Failed while displaying area tested (video RAM).
DSP4	SRAM Test Timeout; test started but never completed.
DSP5	SRAM Failure; RAM failure during SRAM test.

3.6.2.1.2 (O) ROM TEST

This test reads the configuration bytes of the operating system to determine the version, and language/country. All bytes from the operating system ROMs are then read and the checksums are calculated. These sums are then displayed. Finally, for each ROM a CRC is taken and compared with the word in the highest address location.

The test fails if the CRC calculated does not match the CRC found in the high address word. Incorrect CRC's are indicated by a message. If an error is displayed, replace the corresponding ROM.

NOTE: New revisions of TOS will not cause this test to fail since the calculated CRC is compared with a value found in the new TOS ROM's and is independent of a fixed lookup table.

3.6.2.1.3 (M) MIDI TESTS

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

MIDI Error Codes

M0	Data not received. Indicates a broken data path.
M1	Write/Read data mismatch. The data written was not the same as the data read.
M2	Input frame error. Noisy signal.
M3	Input parity error. Noisy signal.
M4	Input data overrun. The 6850 received a byte before the previous byte was read. The MFP may not be responding to the interrupt request.

3.6.2.1.4 (S) SCC SERIAL PORT

The SCC Serial Port diagnostic tests the SCC chip, serial port, and LAN port for several functions. Internal loopback polled (async), break (test ext loopback), external loopback polled (async), modem control lines, and external loopback interrupt (async).

SCC Serial Port Error Codes

Port A Errors:

SCC A internal loopback: Transmitter time-out	Transmitter failed.
SCC A internal loopback: Receiver time-out	Receiver failed.
SCC A internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC A internal loopback: Framing error	Incorrect time between start and stop bits.
SCC A internal loopback: Parity error	Input data had incorrect parity.
SCC A internal loopback: Data compare	Data read was not what was sent.
Port A has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.
LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON	The Carrier detect signal is active without a request to send.
LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING	The request to send signal is on but no carrier is active.
Port A async mode: Transmitter time-out	Transmitter failed.
Port A async mode: Receiver time-out	Receiver failed.
Port A async mode: Overrun	A byte was received before the CPU read the previous byte.
Port A async mode: Framing error	Incorrect time between start and stop bits.
Port A async mode: Parity error	Input data had incorrect parity.
Port A async mode: Data compare	Data read was not what was sent.
Port A modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port A modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port A modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

Port B Errors:

SCC B internal loopback: Transmitter time-out	Transmitter failed.
SCC B internal loopback: Receiver time-out	Receiver failed.
SCC B internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC B internal loopback: Framing error	Incorrect time between start and stop bits.
SCC B internal loopback: Parity error	Input data had incorrect parity.
SCC B internal loopback: Data compare	Data read was not what was sent.
Port B has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.
LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON	The Carrier detect signal is active without a request to send.
LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING	The request to send signal is on but no carrier is active.
Port B async mode: Transmitter time-out	Transmitter failed.
Port B async mode: Receiver time-out	Receiver failed.
Port B async mode: Overrun	A byte was received before the CPU read the previous byte.
Port B async mode: Framing error	Incorrect time between start and stop bits.
Port B async mode: Parity error	Input data had incorrect parity.
Port B async mode: Data compare	Data read was not what was sent.
Port B modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port B modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port B modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

SCC Interrupt Errors:

SCC interrupt error: Transmitter time-out	Transmitter failed.
SCC interrupt error: Receiver time-out	Receiver failed.
SCC interrupt error: Overrun	A byte was received before the CPU read the previous byte.
SCC interrupt error: Framing error	Incorrect time between start and stop bits.
SCC interrupt error: Parity error	Input data had incorrect parity.
SCC interrupt error: Data compare	Data read was not what was sent.
No Tx interrupt	A transmit command was issued but no interrupt occurred.
No Rx interrupt	A receive command was issued but no interrupt occurred.

3.6.2.1.5 (T) TIMING

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the timing for VSYNC and HSYNC, and the video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run. There are two tests which check the bus timing for the AJAX and PSG chips. An error message is printed to the screen, then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

Timing Test Error Codes

T0 MFP timer error. One or more of the four timers in the MFP did not generate an interrupt on counting down.
T1 Vertical Sync. VIDEL is not generating vertical sync in the required time period.
T2 Horizontal Sync. VIDEL is not generating horizontal sync in the required time period.
T3 Display Enable. VIDEL is not generating DE output or the MFP is not generating an interrupt.
T4 Video Counter Error. The COMBO IC is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.
T5 PSG Bus Error. The PSG chip is defective.
T6 AJAX Bus Error. The AJAX chip is defective.

3.6.2.1.6 (I) SCSI DMA

The SCSI port is tested by attaching a SCSI hard disk to the external connector. This disk must be set for unit 0, device 0 and have it's terminating resisters installed. No asumption is made about the number of SCSI masters on the bus, so therefore all disk accesses will be done by arbitration. The SCSI interface is tested in DMA as well as CPU mode. Testing is done non-destructivly at block zero on the hard disk. Reads and writes are executed using both the short and long commands. The test sequence is as follows:

1. Send the reset command

2. Read one 512 byte block from block zero on the hard disk into RAM using the read short command.

3. Write the same 512 byte block back to block zero on the hard disk using the write short command.

4. Read the 512 byte block once more from block zero on the hard disk into a new memory location using the read short command.

5. Compare the two RAM buffers for data integrity.

6. Read one 32 Kbyte block from block zero on the hard disk into RAM using the read extended command.

7. Write the same 32 Kbyte block back to block zero on the hard disk using the write extended command.

8. Read the 32 Kbyte block once more from block zero on the hard disk into a new memory location using the read extended command.

9. Compare the two RAM buffers for data integrity.

10. Using the DMA controller read, write, and read again 64 Kbytes into two different RAM buffers (as above) using the SCSI extended commands.

11. Compare memory for data integrity and DMA over and under shoot outside the RAM buffers.

SCSI Error Messages

ERROR - SCSI STATUS CODE - XX	SCSI controller has reported error number XX
ERROR - CANNOT SELECT SCSI DISK	Cannot win arbitration for SCSI bus
ERROR PRG MODE - READ AND WRITE BUFFERS DO NOT COMPARE	Data in the two RAM buffers are not the same
ERROR DMA MODE - 5380 OR SCSI DISK IS NOT RESPONDING	An attempt to poll the SCSI drive failed
ERROR DMA MODE - READ AND WRITE BUFFERS DO NOT COMPARE	Data in the two RAM buffers are not the same
ERROR-DMA BLOCK MOVE TIME OUT	DMA block move operation timed out.
ERROR-TIME-OUT-SCSI BUS ALWAYS BUSY	Interrupt not seen by MFP

3.6.2.1.7 (F) FLOPPY DISK

In single test mode, a menu is displayed showing seven options:

1.) Quick test.	If the disk is installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not over written. If the disk is not installed, checks to see if the drive is on-line and if its double or single sided. To assure that the drive is correctly tested, the operator should install (menu option 6) before calling the test. Once the test is run, the drive becomes installed, and will be displayed on the menu screen (below the RAM size).
2.) Read track.	Continuously reads a track, for checking alignment with an analog alignment diskette. The track to be read may be input by the operator. If "Return" is pressed without entering a number, the default is track 40.
3.) Interchangeability test.	Checks to see if a diskette formated on another drive can be read by the installed disk drive.
4.) Disk exerciser.	A more thorough disk test; tests all sectors on the disk for an indefinite period of time.
5.) Copy Protect Tracks.	Tests tracks 80-82, which are used by some software companies for copy protection). Not all manufacturers disk drives will write these tracks. **NOTE: this test is for information only and should not be used to reject a mechanism.**
6.) Test speed.	The rotational speed of the drive is tested and displayed on the screen as the period of rotation. The acceptable range is 196-204 milliseconds. The highest and lowest values measured are displayed. The test stops when any key is pressed.
7.) Install disk.	Specify what type of disk to test.

One additional test which can be performed is testing the write protect detection. Slide the write protect tab to the protected position, and run test #1. You should see "F5 Write protected" displayed if the drive has been installed, or "Unable to write disk" displayed if the drive has not been installed.

If more than one test cycle is selected from the main menu, the floppy menu will not appear, but the Quick Test will be selected automatically.

Floppy Test Error Codes

No floppy connected	The controller cannot read index pulses. Indicates the cable may be improperly connected, or the drive has no power, or the drive is faulty.
F0	Drive not selected. Drive was installed, but failed attempting restore (seek to track 0).

The general error messages "Error Writing" (or reading or formatting), are combined with a more specific error message, e.g., "F9 CRC error".

F4	Seek error. Error occurred during a seek.
F5	Write protected. Indicates the floppy is write protected.
F6	Read compare error. Data read from the disk was not what was supposed to be written.
F7	DMA error. DMA Controller could not respond to a request for DMA.
F8	DMA count error. Amount of bytes transferred is not correct.
F9	CRC error. The floppy controller has flaged a CRC error.
FA	Record not found. The floppy could not read a sector header.
FB	Side select error–single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.
FC	Lost data. Data was transferred to the AJAX chip faster than the AJAX could transfer to the DMA Controller.
FD	Drive not ready. The format/write/read operation timed-out.

3.6.2.1.8 (P) PRINTER/JOY/GAME

The port test fixture is used to test the parallel printer port and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU. The game controller port test simulates joystick direction input, fire button input, paddle controller input, and light gun inputs. The FALCON30 (STE) game port test fixture uses the joystick outputs and control lines from the port test fixture to generate the signals input to the FALCON30.

Printer/Joystick Error Codes

P0 Printer port error. Data read from the printer port was not what was written.

P1 Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected.

J0 Joystick Port 0. The keyboard input is not functioning.

J1 Joystick Port 1. The keyboard input is not functioning.

J2 Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, or keyboard-CPU communication line.

J3 Left button input. Not seen by the test board.

J4 Right button input. Not seen by the test board.

J5 Aux Joystick Direction. Game controller port (J500, J501) direction bits. U511 is used to drive the input via the test fixture. The hexadecimal data following corresponds to bits read from latches U510 and U512, where a one indicates an error. For example, 0002 indicates an error at J500 pin 3.

J6 Aux Fire Button. Fire buttons are read from U509. Signal is driven via the test fixture from the output of U511.

J7 Paddle. The inputs are driven by either 5V/100 ohms or 5V/1M on the test fixture. This current charges the RC network on the FALCON30, varying the output pulse of the LM556.

J8 Light gun. The light gun (XPEN) input is toggled at three points on the screen (the video address counter is used to find the position of the screen). The COMBEL should return the X/Y coordinates of the screen position.

3.6.2.1.9 (L) REAL TIME CLK

The test saves the current time and date, and writes a new time, waits one second, and verifies that hours, minutes, seconds, etc. have all rolled over. This procedure is repeated for another date to verify all registers.

Real-Time Clock Error Codes

C0	No Real-Time Clock
C1	Increment Error

3.6.2.1.10 (G) SHORT BLiT

Two tests are available for this chip. The "Short BLiT Test" checks the ability of the BliTTER to move blocks of memory around and perform logical operations on the data. No patterns appear on the screen. If an error is detected, one of the error codes (G1-G12) is displayed.

3.6.2.1.11 (Y) LONG BLiT

In the "Long BLiT Test", a triangle is drawn on the screen and rotated 180 degrees until a rectangle is formed. If a color monitor is used, two identical images will be drawn. If an error occurs, the error code G14 will be displayed.

Corrective action for any error is the same:

a. Verify the jumpers for the BLiT/COMBEL chip are installed correctly.
b. Replace the chip (and if that does not cure the problem, replace the 68030).

Blitter Error Codes:

G1	Halftone RAM (Internal RAM in BLiT portion of COMBEL).
G2	Endmask.
G3	Operation.
G4	Halftone Op.
G5	Skew.
G6	Reverse Bit.
G7	Force Extra Source Read.
G8	Smudge.
G9	X Count.
GA	Y Count.
GB	Time-out.
GC	Address Count
BUS ERROR during BliT Test	Replace COMBEL chip.

3.6.2.1.12 (X) EXPANSION BUS

This test uses the FALCON30 expansion test fixture to verify all address, data, and control lines brought out to the expansion connector.

The test fixture has a minimum of 64k of static RAM and is jumper selectable for 128k. This RAM on power up is addressed at $FC0000 to $FDffff but is software selectable to be remapped to $FA0000 (cartridge ROM space). This means the board can be down loaded with the diagnostic code and then executed from the remapped static RAM for debug purposes. The test fixture can also be configured for installing the diagnostic cartridge EPROMs directly on to the board. Using the ATARI Debug program it will be possible to single step through the diagnostic code to either debug the code itself or for special test applications requiring detailed examination of the FALCON30 hardware as the code is executed.

In the normal configuration the expansion test fixture has on board the following hardware:

1. Control Registers F70000-F70002

2. External blitter F78A00-F78A3F

3. 64k 120 nsec. static RAM FC0000-FCFFFF

The testing is done as follows:

1. A 64k on board RAM test will be executed to test address lines A0-A15 and all 32 data lines for shorts and opens.

2. The address lines (A16-A23) will be tested by reading from the upper 256 addresses and trapping one by one each address read in the address latch register.

3. The on board blitter will, with little modification, execute the FALCON30 blitter tests. This exercises the bus master handshaking lines.

4. Single line tests include the following:

   Priority interrupt, interrupts 1,3,5,and 6.
   Bus Error, halt, reset and 500 kHz.

Expansion Bus Errors

Spurious interrupt 5	A Spurious Interrupt was received on level 5. Check MFP, COMBO, and Interrupt line 5.
Spurious interrupt 1	A Spurious Interrupt was received on level 1. Check MFP, COMBO, and Interrupt line 1.
Spurious interrupt 6	A Spurious Interrupt was received on level 6. Check MFP, COMBO, and Interrupt line 6.
Bus error from int level 6	A Bus Error was asserted while accessing Interrupt Level 6. Check MFP, COMBO, and Interrupt line 6.
Bus error	A Bus Error occurred during testing. Check COMBO.
Spurious Interrupt	A Spurious Interrupt was received during testing. Check MFP, COMBO, and Interrupt lines.
Address Error	An Address Error occurred during testing. Check COMBO, MC68030, and all address lines for shorts or opens.
Halt Test failed	A halt operation failed to take place when programmed. Check COMBO, HALT line, and MC68030.
500 KHZ clock stuck low	The 500 kHz line is stuck. Check COMBO and clock line.
500 KHZ clock stuck high	The 500 kHz line is stuck. Check COMBO and clock line.
printer is not responding...	The printer port did not respond to command. Check printer data line, SDMA, COMBO, and PSG.
Bus error signal stuck low	The Bus Error line is stuck. Check COMBO and Bus Error line.
Bus error signal stuck high	The Bus Error line is stuck. Check COMBO and Bus Error line.
Blitter test failed	Expansion Blitter test failed. Check COMBO, address lines, and data lines.
Expansion port is not connected	Expansion test fixture not installed. Check connection of Expansion Test Fixture.
Address Latch failed at addr\exp\read:	Address Latch Failed. Check COMBO.
Interrupt level 1 failed	Interrupt failed on level 1. Check MFP, COMBO, and Interrupt line 1.
Interrupt level 3 failed	Interrupt failed on level 3. Check MFP, COMBO, and Interrupt line 3.
Interrupt level 5 failed	Interrupt failed on level 5. Check MFP, COMBO, and Interrupt line 5.
Interrupt level 6 failed	Interrupt failed on level 6. Check MFP, COMBO, and Interrupt line 6.
Interrupt priority failed	Interrupt priority test failed. Check MFP, COMBO, and Interrupt lines.
RAM failed addr.write.read:	RAM test failed. Check COMBO and RAM address and data lines.

2.6.1.2.13 DSP Port

This test loads a program into the DSP and then sends it's internal sine wave table out a loopback connector on the DSP port.

NOTE: The loopback connector cannot have any long signal paths or the test will fail intermittently.

DSP Error Codes

DSP0 - DSP Not Executing Program	DSP not responding
DSP1 - SSI Test Timeout	Serial Port Timeout
DSP2 - SSI Loopback Timeout	Data not completing loopback
DSP3 - SSI Bad Data	Data mismatch after loopback

3.6.2.2 OPERATOR TESTS

The Audio, Video, Keyboard, and Hard disk tests have few error messages. The operator generally determines if the outputs are acceptable.

3.6.2.2.1 (A) AUDIO

Audio is tested in several stages and requires an oscilloscope, a microphone in/speaker out loopback cable, and a digital sound loopback connector.

3.6.2.2.1.1 PSG SOUND

This test is used to test the programmable sound generator channels. This PSG output is routed to the CODEC IC device where it is then conditioned by the Tone and Volume controls sent via the SDMA chip. An oscilloscope attached to the Headphone jacks can observe this audio output from the CODEC. The audio sound is a low to high frequency sweep. The sound should be audible through out the sweep range without a drop off in volume. As one cycle of each channel is performed a massage will identify which channel is being exercised (A, B, or C).

DMA sound out is tested next. A table in ROM will be used to generate a sine wave and the output is then varied in the CODEC chip as to rate and volume level. There are four parts in the test set. At the start of each test a message will be displayed; the test cycle started and repeated until the space bar is depressed. The four tests are as follows:

3.6.2.2.1.2 1KHz MONO TONE

1. Mono 1kHz at 4 sample rates, 5 volume levels

3.6.2.2.1.3 1KHz/500 Hz STEREO TONES

2. Stereo 1k/500HZ at 4 sample rates, 5 volume levels

3.6.2.2.1.4 TREBLE ATTENUATION

3. Mono 50 Hz from -12dB attenuation to +12dB

3.6.2.2.1.5 BASS ATTENUATION

4. Mono 12 kHz from -12dB attenuation to +12dB

Using the space bar, the operator should step through the 1 kHz tests and treble, bass attenuation tests; monitoring both output connectors for 4 volts (+/- .2 volts) peak to peak with an oscilloscope.

The data paths and the remaining untested portions of the CODEC and the sound SDMA in/out are tested last.

Using a template in memory a sine wave is generated by The SDMA chip and routed out it's four wire sound data output bus to the digital sound connector. An external loopback plug will reroute the digital data back to the four wire sound data input bus. The SDMA chip will in turn store this new data back into memory. The output data is then compared with the input data. A percentile correct message will then be displayed. This message will be in 10 percent increments. I.E. Less then 10% or greater than 10,20,30...percent.

To complete the testing the digital sound loopback connector must be removed and two microphone/headphone loopback cables installed. The analogue path from/to the CODEC chip and the four wire sound data in/out bus connection will now be tested.

This is done in two stages. First, using the above same template in memory a sine wave is generated by the SDMA chip and routed out it's four wire sound data output bus to the CODEC data in bus. This data is transferred internally in the CODEC to it's ADC channel out bus. The SDMA chip will in turn receive this data via it's 4 wire sound data input bus and then store this new data back into memory. The output data is then compared with the input data. A percentile correct message will then be displayed. This message will be in 10 percent increments. I.E. Less then 10% or greater than 10,20,30...percent.

The last stage of the audio test uses the data template again and the same 4 wire path to/from the SDMA and CODEC chip. However, the data will be routed out the CODEC through the external loopback cables and back to CODEC before reaching the sound SDMA. The percentile check will be made and the information displayed as before.

3.6.2.2.2 (V) VIDEO

The system should be started with an STE color monitor or VGA monitor plugged in. Both monitors will work for most tests. Starting with an STE monitor is required for the Video Monitors test. The STE monitor will be slightly more compatible and should be used if a choice is available.

The VGA monitor is recommended for running the VGA Mode Test. After running the tests, the submenu background will be black to signify a VGA monitor. Returning to the main menu will restore the screen background color.

When the Video Diagnostic is selected a menu will appear as follows:

Video Test Submenu

C Color Test
V VGA Mode Test
M Video Monitors Test

Enter Letter:

3.6.2.2.2.1 Color Test

This is the same as the old STE color test. It can be viewed on the monitor the system was started with, either color or VGA. The test screen appears as a set of R,G,B color bars on the left half, and a rainbow of colors in a block on the right half. The system is ok if all colors are in the bars, and the rainbow colors are the same as a good system.

Note that the color bars are each one DAC bit. If one is missing, check connections to the DAC.

3.6.2.2.2.2 Video Monitors Test

This tests the Videl, the TV modulator, and the other video output circuitry. This test should be run with an RS232 terminal attached so all messages will be shown.

The test starts with the color monitor attached and runs four separate tests. Note that only three screens are displayed, and one TV picture. The SPACE bar is used to increment from one test to the next. **If you press ESC instead of SPACE, the rest of the test will be skipped and the video test menu will return after a color monitor is connected.**

Screen 1: A set of R,G,B color bars on the left half, and a rainbow of colors in a block on the right half. The system is ok if all colors are in the bars, and the rainbow colors are the same as a good system.

Note that the color bars are each one DAC bit. If one is missing, check connections to the DAC. After the test completes connect a TV to the modulator connector and verify proper output. It should look the same as the color test.

Screen 2: Connect a monochrome monitor and press SPACE to advance to the monochrome test. A black screen with white blocks, alternating to a white screen with black blocks (same as old STe Hires test). After verifying monochrome output, connect a VGA monitor and again press SPACE.

Screen 3: A black screen with crossed white lines, (vertical and horizontal centered, diagonal shifted left) a set of color bars on the right, just left of the color bars, a white block with black lines through it, and the contents of the Sparrow palette in a 16x16 square on the left.

The system is ok if the screen is stable, the color bars are of increasing intensity for each color, and in the order G,B,R from top down.
The system has a problem if the colors are in the wrong order, are mixed, or if the lines or blocks are not steady and clear.

Note that the color bars are each one DAC bit. If one is missing, check connections to the DAC.

After checking the VGA output, connect the color monitor again and press SPACE to return to the video test menu.

3.6.2.2.2.3 VGA Modes Test

This tests more of the Videl circuits by displaying several different video modes on a VGA monitor. Again, an RS232 terminal should be connected in order to recieve the test prompts

The first screen is A black screen with crossed white lines, (vertical and horizontal centered, diagonal shifted left) a set of color bars on the right, just left of the color bars, a white block with black lines through it, and the contents of the Sparrow palette in a 16x16 square on the left.

The system is ok if the screen is stable, the color bars are of increasing intensity for each color, and in the order G,B,R from top down.

The system has a problem if the colors are in the wrong order, are mixed, or if the lines or blocks are not steady and clear.

Note that the color bars are each one DAC bit. If one is missing, check connections to the DAC.

The second screen tests 320 x 480 XGA.

NOTE: The second screen does not work on rev. 1 combels and should be skipped by pressing 'B' instead of space after the first screen. The system will most likely crash otherwise.

The third screen tests 640 x 200 STE modes and shows the video test menu screen while changing the background colors. There should be four of each color, in order: dim, bright, less, less.. if there are not, there are problems with the STE palette.

3.6.2.2.3 (K) KEYBOARD

Two types of tests are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). The key will also be displayed in the lower half of the screen. The mouse buttons and four directions are also shown on the screen. Connect the mouse and move in any direction and the arrow will flicker. Any key clicks while the mouse is moving indicates a short. **NOTE: It is possible, if pressing keys very rapidly, to leave the representation of the key on screen in a depressed state. This does not indicate a problem with the hardware.**

The self-test checks communication between the CPU and the keyboard microcomputer, checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

Keyboard Error Codes

K0 Stuck key. A key closure was detected while the keyboard self test was executing.

K1 Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time.

K2 Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status.

3.6.2.2.4 (H) IDE HARD DISK

The IDE Hard Disk test will test the read and write capability of the IDE hard disk. It also tests the DMA channel connected to the hard disk. The test starts by reading and saving the information on cylinder 0. The test then begins a loop where the write buffer is filled with test data. The data is written to cylinder 0 of the hard disk through the DMA channel. The diagnostic then checks for, and displays, any controller errors logged. The read buffer is then cleared and the data in cylinder 0 is put in the read buffer. The controller is again checked for errors. Next the diagnostic checks sthatthe DMA register counted to zero. If not an error message is displayed. Next the buffers are compared and checked for spray. If an error has occurred it is displayed. This loop is repeated until the ESC key is depressed. After the ESC key is pressed the saved cylinder 0 data is written back to the hard disk.

IDE Error Messages

Read error on sector
Write error on sector
Data compare error (wrote, read, hex offset)
Controller not responding
Operation timed-out
Command error
Status =
DMA count error
Error restoring data
DMA address error – Data written outside data buffers
error on command access of disk
reading buffer
failed read of original data from disk
read buffer full - start next cycle
failed writing test data to disk
failed reading test data to disk

3.7 ERROR CODES QUICK REFERENCE

This is a brief summary of all error codes which may occur when running the diagnostic.

INITIALIZATION (Errors occurring before the title and menu appear)

I1	RAM data line is stuck.
I2	RAM disturbance. Location is altered by write to another location.
I3	RAM addressing. Wrong location is being addressed.
I4	MMU error. No DTACK after RAM access.
I5	RAM sizing error. Uppermost address fails.
I6	Bus Error handling failed. Bus Error occurred (on purpose), but caused a crash (e.g. system was unable to read the vector from RAM).
I7	Bus Error not detected. COMBEL not asserting Bus Error or the signal is not reaching the 68030.

EXCEPTIONS (may occur at any time)

E1-E5	not used
E6	Autovector error. IPL0 is grounded or 68000 is bad.
E7	Spurious interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.
E8	Internal Exception (generated by 68030).
E9	Bad Instruction Fetch.
EA	Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceded by a bus error or bad instruction fetch.
EB	Bus error. Generated internally by the 68000 or externally by COMBEL. Usually caused by device not responding. Displays the address of the device being accessed.

RAM & SRAM

R0	Low memory failed while setting up to run test.
R1	Failed walking 1s or 0s.
R2	Failed address (counting pattern).
R3	Failed 64k boundary test. Probable failure in Memory Controller.
R4	Failed while displaying area tested (video RAM).
DSP4	SRAM Test Timeout; test started but never completed.
DSP5	SRAM Failure; RAM failure during SRAM test.

MIDI

M0	Data not received. Indicates a broken data path.
M1	Write/Read data mismatch. The data written was not the same as the data read.
M2	Input frame error. Noisy signal.
M3	Input parity error. Noisy signal.
M4	Input data overrun. The 6850 received a byte before the previous byte was read. The MFP may not be responding to the interrupt request.

SERIAL PORT

Port A Errors:

SCC A internal loopback: Transmitter time-out	Transmitter failed.
SCC A internal loopback: Receiver time-out	Receiver failed.
SCC A internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC A internal loopback: Framing error	Incorrect time between start and stop bits.
SCC A internal loopback: Parity error	Input data had incorrect parity.
SCC A internal loopback: Data compare	Data read was not what was sent.
Port A has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.
LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON	The Carrier detect signal is active without a request to send.
LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING	The request to send signal is on but no carrier is active.
Port A async mode: Transmitter time-out	Transmitter failed.
Port A async mode: Receiver time-out	Receiver failed.
Port A async mode: Overrun	A byte was received before the CPU read the previous byte.
Port A async mode: Framing error	Incorrect time between start and stop bits.
Port A async mode: Parity error	Input data had incorrect parity.
Port A async mode: Data compare	Data read was not what was sent.
Port A modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port A modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port A modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

Port B Errors:

SCC B internal loopback: Transmitter time-out	Transmitter failed.
SCC B internal loopback: Receiver time-out	Receiver failed.
SCC B internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC B internal loopback: Framing error	Incorrect time between start and stop bits.
SCC B internal loopback: Parity error	Input data had incorrect parity.
SCC B internal loopback: Data compare	Data read was not what was sent.
Port B has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.
LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON	The Carrier detect signal is active without a request to send.
LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING	The request to send signal is on but no carrier is active.
Port B async mode: Transmitter time-out	Transmitter failed.
Port B async mode: Receiver time-out	Receiver failed.
Port B async mode: Overrun	A byte was received before the CPU read the previous byte.
Port B async mode: Framing error	Incorrect time between start and stop bits.
Port B async mode: Parity error	Input data had incorrect parity.
Port B async mode: Data compare	Data read was not what was sent.
Port B modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port B modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port B modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

SCC Interrupt Errors:

SCC interrupt error: Transmitter time-out	Transmitter failed.
SCC interrupt error: Receiver time-out	Receiver failed.
SCC interrupt error: Overrun	A byte was received before the CPU read the previous byte.
SCC interrupt error: Framing error	Incorrect time between start and stop bits.
SCC interrupt error: Parity error	Input data had incorrect parity.
SCC interrupt error: Data compare	Data read was not what was sent.
No Tx interrupt	A transmit command was issued but no interrupt occurred.
No Rx interrupt	A receive command was issued but no interrupt occurred.

TIMING

T0 MFP timer error. One or more of the four timers in the MFP did not generate an interrupt on counting down.
T1 Vertical Sync. VIDEL is not generating vertical sync in the required time period.
T2 Horizontal Sync. VIDEL is not generating horizontal sync in the required time period.
T3 Display Enable. VIDEL is not generating DE output or the MFP is not generating an interrupt.
T4 Video Counter Error. The COMBO IC is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.
T5 PSG Bus Error. The PSG chip is defective.
T6 AJAX Bus Error. The AJAX chip is defective.

BLITTER

G1	Halftone RAM (Internal RAM in BLiT portion of COMBEL).
G2	Endmask.
G3	Operation.
G4	Halftone Op.
G5	Skew.
G6	Reverse Bit.
G7	Force Extra Source Read.
G8	Smudge.
G9	X Count.
GA	Y Count.
GB	Time-out.
GC	Address Count
BUS ERROR during BliT Test	Replace COMBEL chip.

REAL-TIME CLOCK

C0	No Real-Time Clock
C1	Increment Error

SCSI

ERROR - SCSI STATUS CODE - XX	SCSI controller has reported error number XX
ERROR - CANNOT SELECT SCSI DISK	Cannot win arbitration for SCSI bus
ERROR PRG MODE - READ AND WRITE BUFFERS DO NOT COMPARE	Data in the two RAM buffers are not the same
ERROR DMA MODE - 5380 OR SCSI DISK IS NOT RESPONDING	An attempt to poll the SCSI drive failed
ERROR DMA MODE - READ AND WRITE BUFFERS DO NOT COMPARE	Data in the two RAM buffers are not the same
ERROR-DMA BLOCK MOVE TIME OUT	DMA block move operation timed out.
ERROR-TIME-OUT-SCSI BUS ALWAYS BUSY	Interrupt not seen by MFP

KEYBOARD

K0 Stuck key. A key closure was detected while the keyboard self test was executing.

K1 Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time.

K2 Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status.

IDE

Read error on sector
Write error on sector
Data compare error (wrote, read, hex offset)
Controller not responding
Operation timed-out
Command error
Status =
DMA count error
Error restoring data
DMA address error – Data written outside data buffers
error on command access of disk
reading buffer
failed read of original data from disk
read buffer full - start next cycle
failed writing test data to disk
failed reading test data to disk

PRINTER AND JOYSTICK PORTS

P0 Printer port error. Data read from the printer port was not what was written.

P1 Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected.

J0 Joystick Port 0. The keyboard input is not functioning.

J1 Joystick Port 1. The keyboard input is not functioning.

J2 Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, or keyboard-CPU communication line.

J3 Left button input. Not seen by the test board.

J4 Right button input. Not seen by the test board.

J5 Aux Joystick Direction. Game controller port (J500, J501) direction bits. U511 is used to drive the input via the test fixture. The hexadecimal data following corresponds to bits read from latches U510 and U512, where a one indicates an error. For example, 0002 indicates an error at J500 pin 3.

J6 Aux Fire Button. Fire buttons are read from U509. Signal is driven via the test fixture from the output of U511.

J7 Paddle. The inputs are driven by either 5V/100 ohms or 5V/1M on the test fixture. This current charges the RC network on the FALCON30, varying the output pulse of the LM556.

J8 Light gun. The light gun (XPEN) input is toggled at three points on the screen (the video address counter is used to find the position of the screen). The COMBEL should return the X/Y coordinates of the screen position.

FLOPPY DISK DRIVE

No floppy connected	The controller cannot read index pulses. Indicates the cable may be improperly connected, or the drive has no power, or the drive is faulty.
F0	Drive not selected. Drive was installed, but failed attempting restore (seek to track 0).

The general error messages "Error Writing" (or reading or formatting), are combined with a more specific error message, e.g., "F9 CRC error".

F4	Seek error. Error occurred during a seek.
F5	Write protected. Indicates the floppy is write protected.
F6	Read compare error. Data read from the disk was not what was supposed to be written.
F7	DMA error. DMA Controller could not respond to a request for DMA.
F8	DMA count error. Amount of bytes transferred is not correct.
F9	CRC error. The floppy controller has flaged a CRC error.
FA	Record not found. The floppy could not read a sector header.
FB	Side select error–single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.
FC	Lost data. Data was transferred to the AJAX chip faster than the AJAX could transfer to the DMA Controller.
FD	Drive not ready. The format/write/read operation timed-out.

EXPANSION PORT

Spurious interrupt 5	A Spurious Interrupt was received on level 5. Check MFP, COMBO, and Interrupt line 5.
Spurious interrupt 1	A Spurious Interrupt was received on level 1. Check MFP, COMBO, and Interrupt line 1.
Spurious interrupt 6	A Spurious Interrupt was received on level 6. Check MFP, COMBO, and Interrupt line 6.
Bus error from int level 6	A Bus Error was asserted while accessing Interrupt Level 6. Check MFP, COMBO, and Interrupt line 6.
Bus error	A Bus Error occurred during testing. Check COMBO.
Spurious Interrupt	A Spurious Interrupt was received during testing. Check MFP, COMBO, and Interrupt lines.
Address Error	An Address Error occurred during testing. Check COMBO, MC68030, and all address lines for shorts or opens.
Halt Test failed	A halt operation failed to take place when programmed. Check COMBO, HALT line, and MC68030.
500 KHZ clock stuck low	The 500 kHz line is stuck. Check COMBO and clock line.
500 KHZ clock stuck high	The 500 kHz line is stuck. Check COMBO and clock line.
printer is not responding...	The printer port did not respond to command. Check printer data line, SDMA, COMBO, and PSG.
Bus error signal stuck low	The Bus Error line is stuck. Check COMBO and Bus Error line.
Bus error signal stuck high	The Bus Error line is stuck. Check COMBO and Bus Error line.
Blitter test failed	Expansion Blitter test failed. Check COMBO, address lines, and data lines.
Expansion port is not connected	Expansion test fixture not installed. Check connection of Expansion Test Fixture.
Address Latch failed at addr\exp\read:	Address Latch Failed. Check COMBO.
Interrupt level 1 failed	Interrupt failed on level 1. Check MFP, COMBO, and Interrupt line 1.
Interrupt level 3 failed	Interrupt failed on level 3. Check MFP, COMBO, and Interrupt line 3.
Interrupt level 5 failed	Interrupt failed on level 5. Check MFP, COMBO, and Interrupt line 5.
Interrupt level 6 failed	Interrupt failed on level 6. Check MFP, COMBO, and Interrupt line 6.
Interrupt priority failed	Interrupt priority test failed. Check MFP, COMBO, and Interrupt lines.
RAM failed addr.write.read:	RAM test failed. Check COMBO and RAM address and data lines.

DSP Port Error Codes

DSP0 - DSP Not Executing Program	DSP not responding
DSP1 - SSI Test Timeout	Serial Port Timeout
DSP2 - SSI Loopback Timeout	Data not completing loopback
DSP3 - SSI Bad Data	Data mismatch after loopback

SECTION FOUR
DISASSEMBLY/ASSEMBLY

4.1 FALCON030 DISASSEMBLY

Use the following procedure to disassemble the FALCON030. Refer to Assembly Drawings, Section 7.

4.1.1 Top Cover/Keyboard Removal

1. Turn unit upside down.
2. Remove the 4 screws, item 220, from the square holes. Remove the 3 screws, item 240, from the round holes. These fasten the top case to the bottom.
3. Turn the unit upright and remove the top case, item 210.
4. Remove the keyboard, item 200, by unplugging the keyboard harness connector located in the right front corner.

4.1.2 Shield and Speaker Removal

1. Remove the 9 screws, item 80, holding the shield, item 160, and speaker assembly, items 170, 180, 1nd 190, in place.
2. Remove the shield.

4.1.3 Floppy Disk Removal

1. Turn the unit upside down.
2. Remove the 3 screws, item 150, in the round holes.
3. While holding the drive in place turn the unit back over.
4. Lift the disk drive, item 120, slightly and unplug the power harness connector and the ribbon cable.
5. Remove the drive, item 120, and standoffs, item 130.

4.1.4 Power Supply Removal

1. Unplug the wire harness connector in the right front corner of the power supply, item 90.
2. Remove the 4 screws, item 80, at corners of power supply.
3. Lift the power supply up out of the main assembly.

4.1.5 Memory Board Removal

1. Lift the memory board, item 110, out of the unit.

4.1.6 Removal of Main Assembly from Bottom Case

1. Remove three screws, item 80, from the front of the shield/printed circuit board assembly.
2. If power supply has not already been removed, remove the power supply.
3. Lift the assembly up from the front and pull forward.

4.1.7 Removal of Upper Shield from Printed Circuit Board

1. Remove the 6 screws, item 50, from the upper shield, item 40.
2. Remove the upper shield, item 40.

   Note: Now that the major components are exposed, this is a convenient configuration for troubleshooting. The keyboard and disk drive may be re-connected and placed off to the side if those components are needed.

3. Lift printed circuit assembly, item 30, away from the PCB insulator, item 20, and bottom shield, item 10.

4.2 FALCON030 RE-ASSEMBLY

1. Place insulation panel, item 20, on Bottom Shield, item 10.
2. Place Main Board, item 30, on top of Bottom Shield, item 10, over insulator panel item 20.
3. Replace the 6 screws, item 50, in the upper shield, item 40.
4. Place assembly in lower plastic case.

5. Replace the three screws, item 80, in the front of the shield/printed circuit board assembly.

6. Replace the memory board, item 110, in the unit.

7. Replace the power supply in the main assembly.

8. Replace the 4 screws, item 80, at corners of power supply.

9. Plug the wire harness connector in the right front corner of the power supply, item 90, into the main PCB.

10. Replace the drive, item 120, and standoffs, item 130.

11. Lift the disk drive, item 120, slightly and plug in the power harness connector and the ribbon cable.

12. While holding the drive in place turn the unit over.

13. Replace the 3 screws, item 150, in the round holes.

14. Turn the unit back over.

15. Replace the shield.

16. Replace the 9 screws, item 80, holding the shield, item 160, and speaker assembly, items 170, 180, 1nd 190, in place.

17. Replace the keyboard, item 200, and plug the keyboard harness connector located in the right front corner.

18. Turn the unit upright and replace the top case, item 210.

19. Replace the 4 screws, item 220, in the square holes. Replace the 3 screws, item 240, in the round holes. These fasten the top case to the bottom.

20. Turn unit upside down.

Warning: It is strongly recommended that the computer be retested once in plastic to make sure that the reassembly was done correctly and there are no shorts to the shield.

SECTION FIVE:
SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section of troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

5.1 DISPLAY PROBLEMS

Symptom	Probable Cause
Black Screen	No power (check LED), bad COMBO IC, bad VIDEL IC. See Section 3.3: Troubleshooting a Dead Unit.
White Screen	VIDEL IC, COMBO IC, SDMA IC, MC68030. Use diagnostic cartridge with terminal connected via RS232 port.
Dots/Bars on Screen	Bad SIMM modile, COMBO IC, VIDEL IC. Use the diagnostic cartridge.
One Color Missing	Video cable or connector. SGC DAC, VIDEL IC. Check signals with oscilloscope.
Monochrome Monitor Fails to Sync but Color Monitor Okay	Verify that the monochrome monitor detect bit is being grounded when monochrome monitor is plugged in. Check MFP GPIP bit 7; replace MFP.
Scrambled Screen	COMBO IC. Use diagnostic cartridge.
TV Output Bad	Modulator, phase locked loop. Trace signal with oscilloscope.

5.2 DISK DRIVE PROBLEMS

Symptom	Probable Cause
Disk Won't Boot	Power supply, AJAX IC, SDMA, PSG chip, IRQ lines shorted to ground. See if Select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check power supply. Swap disk drive or try external drive. If not working, check SDMA Controller and AJAX IC with diagnostic chart.
Disk Won't Format	AJAX IC, SDMA Controller, disk drive.
System Crash after Loading Files	Data on diskette, disk drive, AJAX IC, SDMA, or COMBO IC. Swap diskette, retry. Use diagnostic cartridge to check AJAX IC, SDMA Controller, COMBO IC; replace disk drive.

5.3 KEYBOARD PROBLEMS

Symptom	Probable Cause
Red Screen: Keyboard not responding	Bad keyboard, 6850, MFP.

5.4 MIDI PROBLEMS

Symptom	Probable Cause
Red Screen: MIDI Errors	Bad opto-isolator chip, 6850, inverter (74LS06).

5.5 RS232 PROBLEMS

Symptom	Probable Cause
Red Screen: SCC Error	Bad SCC, 1489 receiver, 1488 driver, or PSG chips, ±12 VDC:DC inverting power supply. See Section 3.12.1.

5.6 PRINTER PORT PROBLEMS

Symptom	Probable Cause
Red Screen: Printer Error	Bad PSG, MFP chips. See Section 3.17.1
Shadow Printing	Bad ASCI port cables, terminator resistors, bad LS244, LS245 drivers.

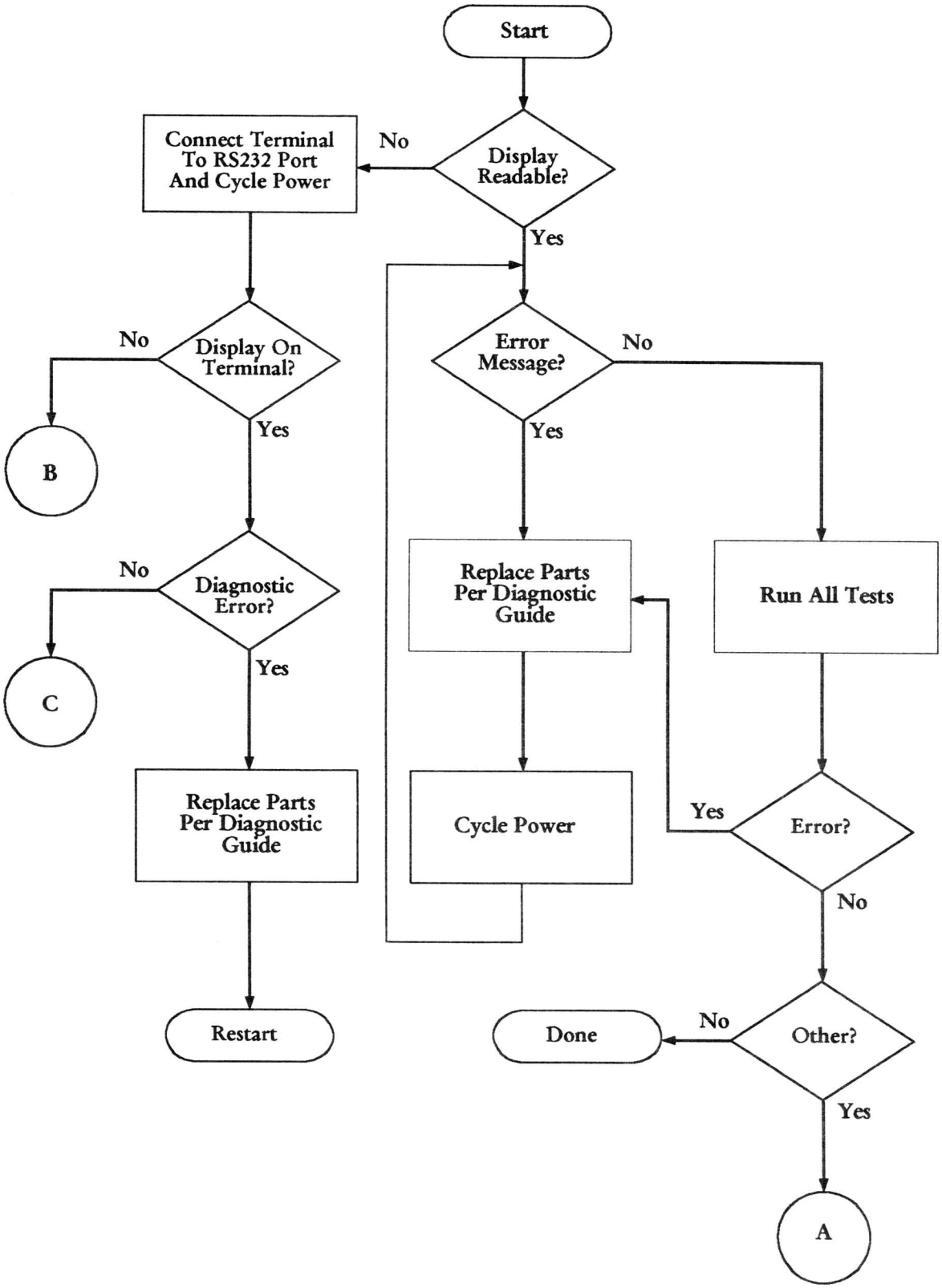
5.7 HARD DISK PORT PROBLEMS

Symptom	Probable Cause
Red Screen: DMA Error	Bad SDMA Controller, COMBO IC, AJAX IC (loading the bus), 5380SCSI Controller. See Section 3.15.1

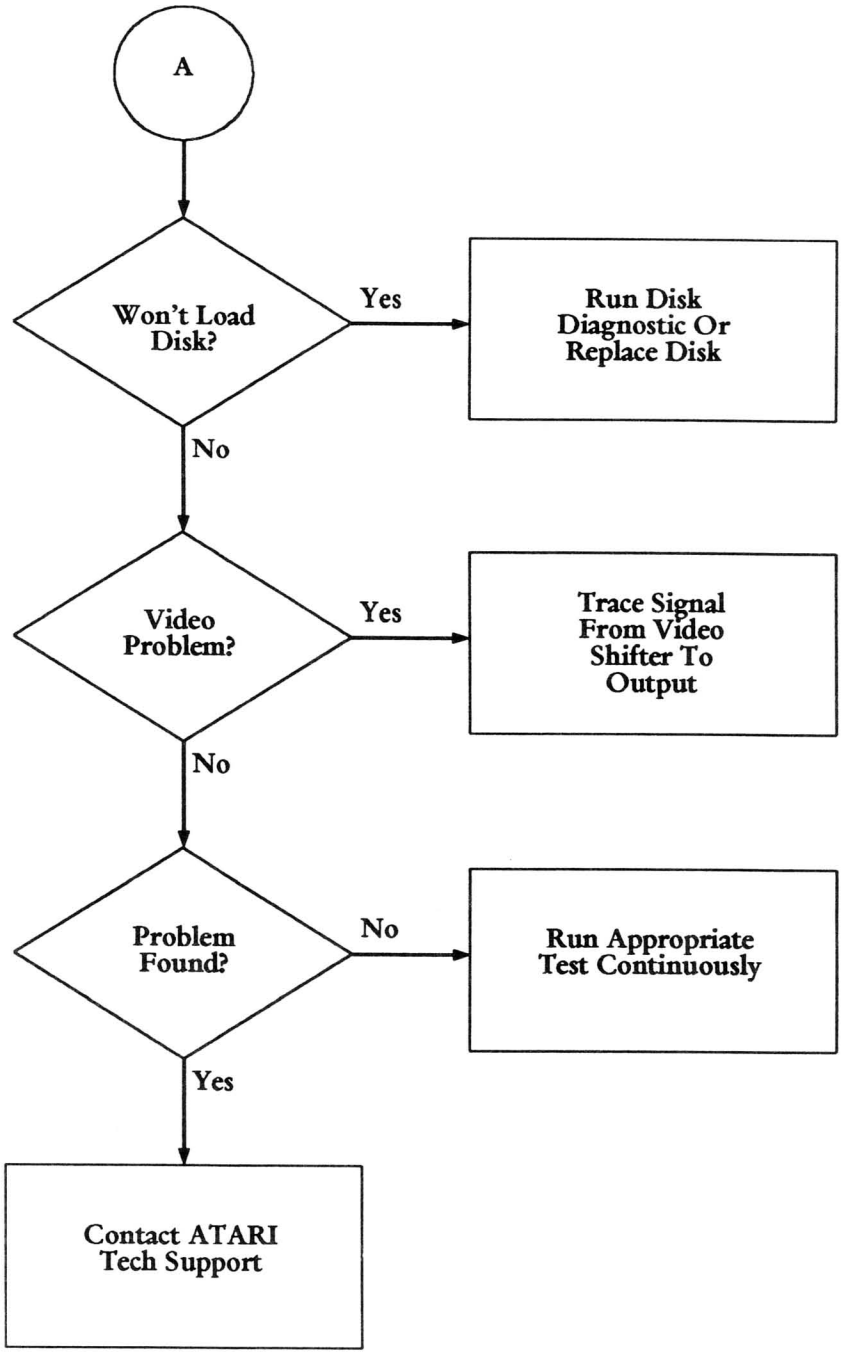
5.8 DMA SOUND

Symptom	Probable Cause
No Sound	+8V regulator, ±supplies, DSP IC, CODEC IC, SDMA IC.

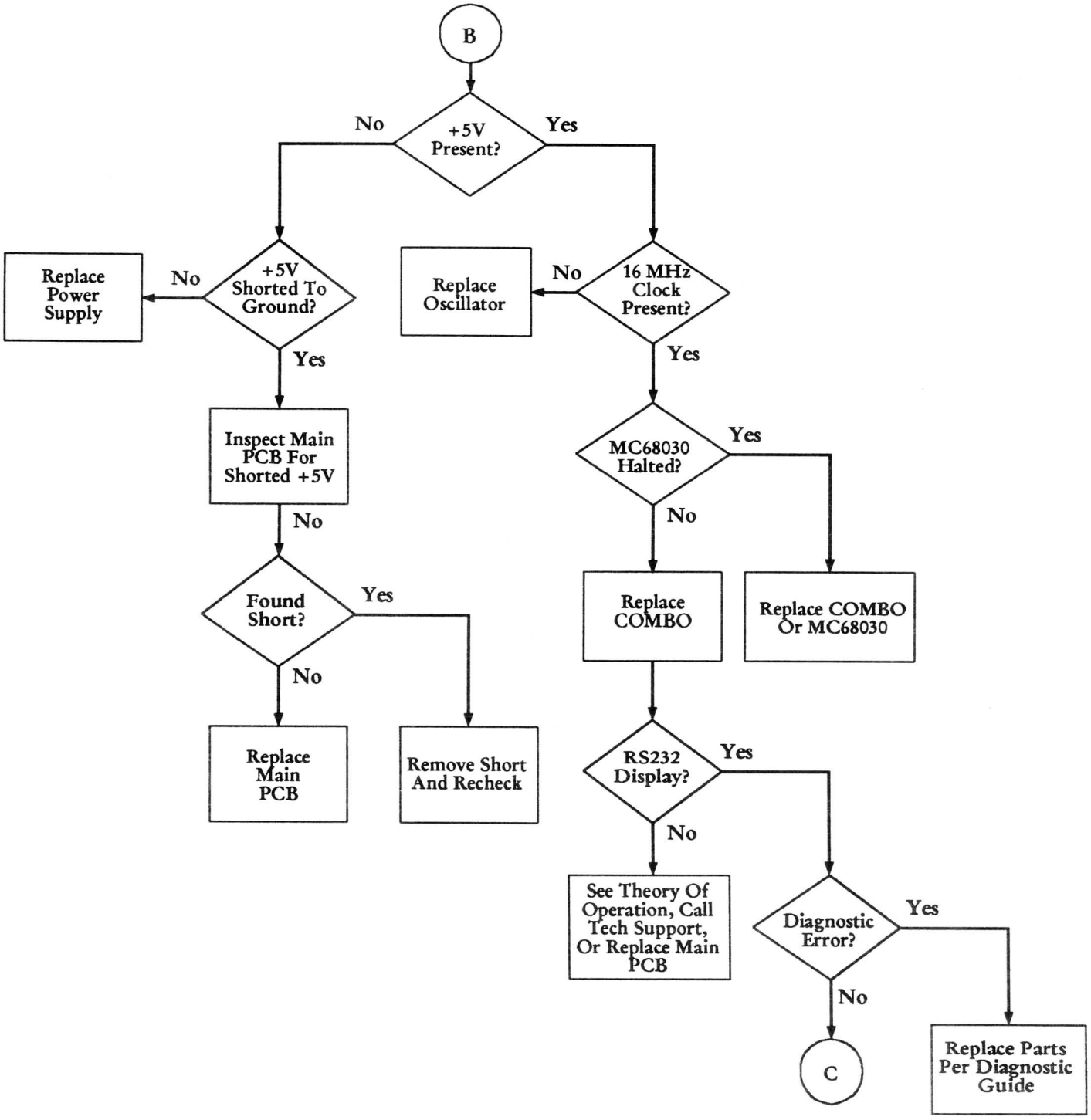
SECTION SIX
DIAGNOSTIC FLOWCHARTS



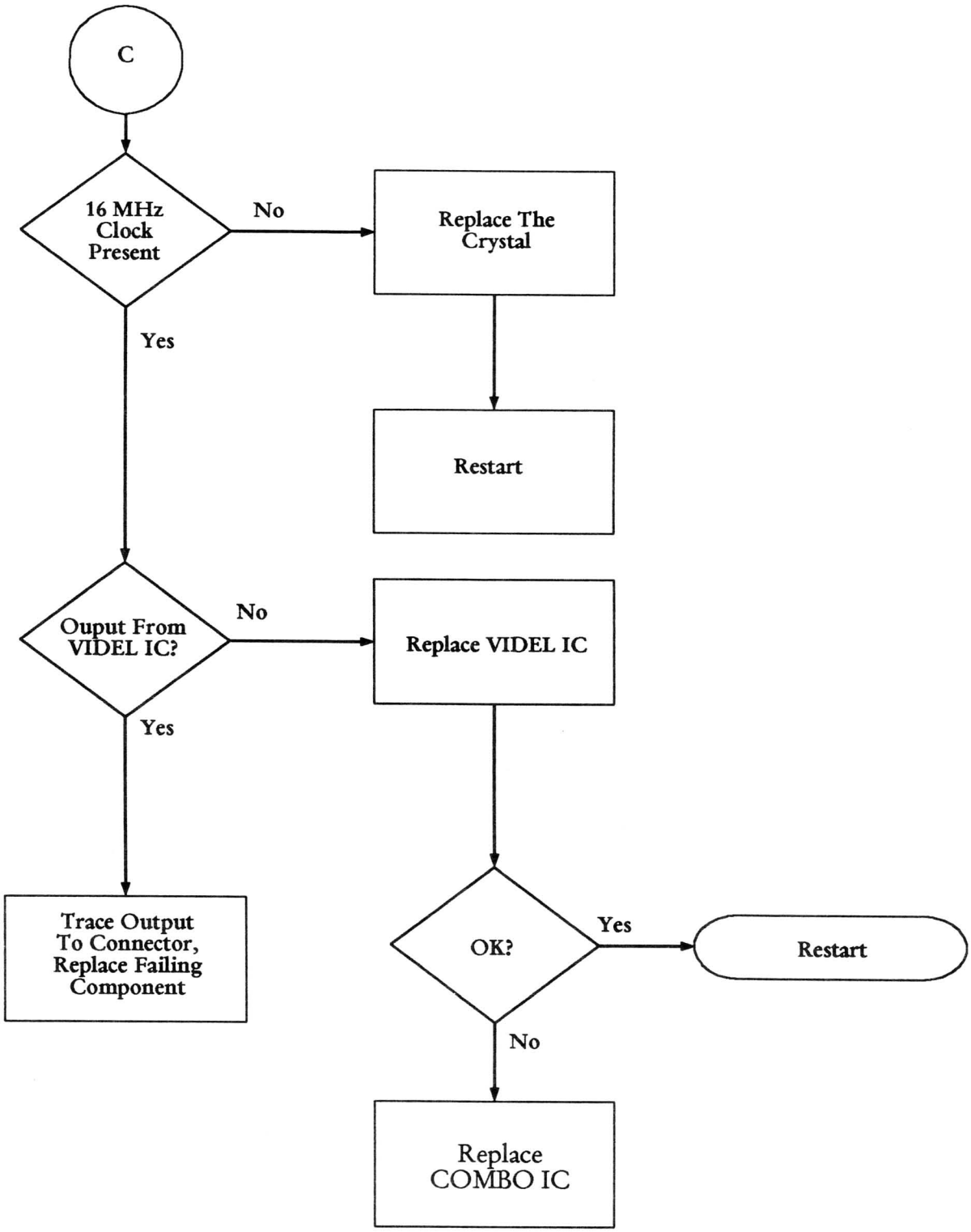
No Error on Diagnostic



No Display on Monitor or Terminal



No Display
No Error



SECTION SEVEN

PARTS LIST AND ASSEMBLY DRAWINGS

Major Subassemblies

Main PCB Assemblies

ITEM	PART NUMBER	DESCRIPTION
30	CA401332-001	ASSY PCB FALCON030 NTSC
30	CA401332-002	ASSY PCB FALCON030 PAL-I
30	CA401332-003	ASSY PCB FALCON030 PAL-B
30	CA401332-004	ASSY PCB FALCON030 PERITEL

Keyboard Assemblies

ITEM	PART NUMBER	DESCRIPTION
200	CA401297-001	K/B FALCON030 W/COP USA
200	CA401297-006	K/B W/COP888 ITA
200	CA401297-003	K/B FX-1 W/COP UK
200	CA401297-004	K/B FX-1 W/COP FRA
200	CA401297-020	K/B W/COP888 SWF
200	CA401297-009	K/B W/COP888 SPA
200	CA401297-012	K/B W/COP888 SWD
200	CA401297-010	K/B COP888 SWG

Mouse Assemblies

ITEM	PART NUMBER	DESCRIPTION
	CA070025-001	Mouse Mitsumi

Disk Drives

ITEM	PART NUMBER	DESCRIPTION
120	C303073-001	FDD 3.5" 2MB FALCON030

POWER SUPPLY

ITEM	PART NUMBER	DESCRIPTION
90	C302866-001	ASSY PSU 117V
90	C302867-001	ASSY PSU 230V

MEMORY

ITEM	PART NUMBER	DESCRIPTION
110	CA401292-001	ASSY PCB 1 MEG DRAM
110	CA401292-002	ASSY PCB 4 MEG DRAM
110	CA401294-001	ASSY PCB 16 MEG DRAM

ROM SETS

ITEM	PART NUMBER	DESCRIPTION
U51	CA401299-001	ASSY TOS FALCON030 USA
U51	CA401299-003	ASSY TOS FALCON030 UK/AUS
U51	CA401299-004	ASSY TOS FALCON030 FRA
U51	CA401299-006	ASSY TOS FALCON030 ITA
U51	CA401299-001	ASSY TOS FALCON030 SPA
U51	CA401299-010	ASSY TOS FALCON030 SWG
U51	CA401299-012	ASSY TOS FALCON030 SWD

INTEGRATED CIRCUITS AND COMPONENTS

PARTS UNIQUE TO PCB FALCON030 NTSC

ITEM	PART NUMBER	DESCRIPTION
Q3	34-2N3904	TRAN 2N3904 3P
R104,105,108	C060629	RES JMPR 0 AX.
C24	C070450-008	CAP ELEC 470UF 35V 20% AX
C36,50	C070499-004	CAP ELEC 100UF 16V 20% AX
U18	C100117	IC 1377 DIP 20P
U4	C100184	RF MODU ST NTSC
DL1	C100209	DELAY LINE 3.58MHZ
L61	C100210	IND COIL VARIABLE 24UH
R106,107,80	C101013-102	RES CHIP 1K OHM 1/10W 5%
R116,117	C101013-122	RES CHIP 1.2K 1/10W 5%
R46	C101013-152	RES CHIP 1.5K 1/10W 5%
R47	C101013-222	RES CHIP 2.2K OHM 1/10W 5%
R70	C101013-562	RES CHIP 5.6K 1/10W 5%
R79	C101013-563	RES CHIP 56K 1/10W 5%
R45	C101021-151	RES 150 5%1/4W 200PPM SMD 3216
R30	C101021-750	RES CHIP,75 1/4W5%
C48	C101212-010	CAP ELEC 1UF 50V 20% AX

PARTS UNIQUE TO PCB FALCON030 NTSC

ITEM	PART NUMBER	DESCRIPTION
C69	C398768-001	CAP MYLAR 1000PF 100V +-5%
C93	C101219-121	CAP CER CHIP 120PF 50V 5% CH
C71	C101220-102	CAP CERA CHIP .001UF 50V 10%
C70,75	C101221-103	CAP CERA CHIP .01UF 50V +80-20
C37,49,60, 61,233	C302904-104	CAP CERA CHIP,0.1UF 50V+80-20%
U65	C303023-005	OSC 32.215905MHZ 8P W/DIS
C51,72,87	C398069-001	CAP TANT 15UF 25V +/-20%

PARTS UNIQUE TO PCB FALCON030 PAL-I

ITEM	PART NUMBER	DESCRIPTION
R108	14-5220	RES CF 22 OHM 1/4W 5%
Q3,7,8,9	34-2N3904	TRAN 2N3904 3P
L112	C017222	IND 1.5UH 10% AX
L111	C017948-08	INDUCTOR, 1UH AX
Y3	C070176	CRYSTAL 32.084988 MHZ
D12,13	C070177	DIODE 1SV69
L105	C070205	IND .27UH 20% AX
C24	C070450-008	CAP ELEC 470UF 35V 20% AX
C224	C070474	CAP TRIMMER 5-30PF
C36,50	C070499-004	CAP ELEC 100UF 16V 20% AX
Y2	C070760	CRYSTAL 4.433618 MHZ 16PF
U18	C100117	IC 1377 DIP 20P
U4	C100185	RF MODU ST PAL I
DL1	C100213	DELAY LINE 4.43MHZ
L61	C100214	IND COIL VARIABLE 14UH
R106,80	C101013-102	RES CHIP 1K OHM 1/10W 5%
R247,254	C101013-104	RES CHIP 100K 1/10W 5%
R240	C101013-105	RES CHIP 1M 1/10W 5%
R107,116,117	C101013-122	RES CHIP 1.2K 1/10W 5%
R46	C101013-152	RES CHIP 1.5K 1/10W 5%
R47	C101013-182	RES CHIP 1.8K 1/10W 5%
R245,253	C101013-222	RES CHIP 2.2K OHM 1/10W 5%
R252	C101013-272	RES CHIP 2.7K 1/10W 5%
R244	C101013-362	RES CHIP 3.6K 1/10W 5%
R246	C101013-431	RES CHIP 430 OHM 1/10W 5%
R258	C101013-472	RES CHIP 4.7K 1/10W 5%
R79	C101013-473	RES CHIP 47K 1/10W 5%
R257	C101013-561	RES CHIP 560 1/10W 5%
R256,70	C101013-562	RES CHIP 5.6K 1/10W 5%
R255	C101013-682	RES CHIP 6.8K 1/10W 5%
R251,45	C101021-151	RES 150 5% 1/4W 200PPM SMD
R30	C101021-750	RES CHIP, 75 1/4W 5%

ITEM	PART NUMBER	DESCRIPTION
C48	C101212-010	CAP ELEC 1UF 50V 20% AX
C236	C101219-080	CAP CERA CHIP,8PF 50V 5% CH
C93	C101219-101	CAP CERA CHIP 100PF 50V 5% CH
C220,221	C101219-200	CAP CERA CHIP 20PF 50V 5% CH
C239	C101219-270	CAP CER CHIP 27PF 50V 5% CH

PARTS UNIQUE TO PCB FALCON030 PAL-I

ITEM	PART NUMBER	DESCRIPTION
C235	C101219-330	CAP CER CHIP 33PF 50V 5%
C237,71	C101220-102	CAP CERA CHIP .001UF 50V 10%
C62,73	C101220-222	CAP CER CHIP .0022UF 50V 10%
C222	C101220-472	CAP CER CHIP 4700PF 50V 10%
C70,75	C101221-103	CAP CERA CHIP .01UF 50V +80-20
C234	C101221-223	CAP CERA CHIP .022UF50V+80-20
U58	C302624-004	IC 74HC04 SOIC 14P
U57	C302889-074	IC 74LS74 SOIC 14P
C37,49,60,61	C302904-104	CAP CERA CHIP,0.1UF 50V+80-20%
C238	C302904-474	CAP CER CHIP .47UF 50V +80-20
C51,72,87	C398069-001	CAP TANT 15UF 25V +/-20% RA
C69	C398768-001	CAP MYLAR 1000PF 100V +-5% RA

PARTS UNIQUE TO PCB FALCON030 PAL-B

ITEM	PART NUMBER	DESCRIPTION
R108	14-5220	RES CF 22 OHM 1/4W 5%
Q3,7,8,9	34-2N3904	TRAN 2N3904 3P
L112	C017222	IND 1.5UH 10% AX
L111	C017948-08	INDUCTOR, 1UH AX
Y3	C070176	CRYSTAL 32.084988 MHZ
D12,13	C070177	DIODE 1SV69
L105	C070205	IND .27UH 20% AX
C24	C070450-008	CAP ELEC 470UF 35V 20% AX
C224	C070474	CAP TRIMMER 5-30PF
C36,50	C070499-004	CAP ELEC 100UF 16V 20% AX
Y2	C070760	CRYSTAL 4.433618 MHZ 16PF
U18	C100117	IC 1377 DIP 20P
U4	C100186	RF MODU ST PAL B
DL1	C100213	DELAY LINE 4.43MHZ
L61	C100214	IND COIL VARIABLE 14UH
R106,80	C101013-102	RES CHIP 1K OHM 1/10W 5%
R247,254	C101013-104	RES CHIP 100K 1/10W 5%
R240	C101013-105	RES CHIP 1M 1/10W 5%
R107,116,117	C101013-122	RES CHIP 1.2K 1/10W 5%
R46	C101013-152	RES CHIP 1.5K 1/10W 5%
R245,253	C101013-222	RES CHIP 2.2K OHM 1/10W 5%
R252,47	C101013-272	RES CHIP 2.7K 1/10W 5%

ITEM	PART NUMBER	DESCRIPTION
R244	C101013-362	RES CHIP 3.6K 1/10W 5%
R246	C101013-431	RES CHIP 430 OHM 1/10W 5%
R258	C101013-472	RES CHIP 4.7K 1/10W 5%
R79	C101013-473	RES CHIP 47K 1/10W 5%
R257	C101013-561	RES CHIP 560 1/10W 5%
R256,70	C101013-562	RES CHIP 5.6K 1/10W 5%
R255	C101013-682	RES CHIP 6.8K 1/10W 5%
R251,45	C101021-151	RES 150 5%1/4W 200PPM SMD
R30	C101021-750	RES CHIP,75 1/4W5%

PARTS UNIQUE TO PCB FALCON030 PAL-B

ITEM	PART NUMBER	DESCRIPTION
C48	C101212-010	CAP ELEC 1UF 50V 20% AX
C236	C101219-080	CAP CERA CHIP,8PF 50V 5%
C93	C101219-101	CAP CERA CHIP 100PF 50V 5%
C220,221	C101219-200	CAP CERA CHIP 20PF 50V 5%
C239	C101219-270	CAP CER CHIP 27PF 50V 5%
C235	C101219-330	CAP CER CHIP 33PF 50V 5%
C71,237	C101220-102	CAP CERA CHIP .001UF 50V 10%
C62,73	C101220-222	CAP CER CHIP .0022UF 50V 10%
C222	C101220-472	CAP CER CHIP 4700PF 50V 10%
C70,75	C101221-103	CAP CERA CHIP .01UF 50V +80-20
C234	C101221-223	CAP CERA CHIP .022UF50V+80-20
U58	C302624-004	IC 74HC04 SOIC 14P
U57	C302889-074	IC 74LS74 SOIC 14P
C37,49,60,61	C302904-104	CAP CERA CHIP,0.1UF 50V+80-20%
C238	C302904-474	CAP CER CHIP .47UF 50V +80-20
C51,72,87	C398069-001	CAP TANT 15UF 25V +/-20%
C69	C398768-001	CAP MYLAR 1000PF 100V +-5%

PARTS UNIQUE TO PCB FALCON030 PERITEL

ITEM	PART NUMBER	DESCRIPTION
Q1	34-2N3904	TRAN 2N3904 3P
D4,7	C060607	DIODE SILICON(SWITCHING)
R33	C101013-103	RES CHIP 10K 1/10W 5%
R31	C101021-101	RES 100 5%1/4W 200PPM SMD
R32	C101021-151	RES 150 5%1/4W 200PPM SMD
C233	C302904-104	CAP CERA CHIP,0.1UF 50V+80-20%
U65	C303023-004	OSC 32.084988MHZ 8P W/DIS

PARTS COMMON TO ALL PCB FACON030

ITEM	PART NUMBER	DESCRIPTION
R74	14-5010	RES CF 1 1/4W 5%
R135	14-54R7	RES CF 4.7 1/4W 5% AX
R8	14-55R1/A	RES CF AX 5.1 1/4W 5%

ITEM	PART NUMBER	DESCRIPTION
D5,6	31-1N4001	DIODE RECTIFIER SILICON
Q5	33-2N3906	TRAN 2N3906 3P
Q2,4,6	34-2N3904	TRAN 2N3904 3P
L27,29,30,32-43, 46-54,56-58,L60, 62-78,80,82,85, 97-99,L5,L102, 104,110,117	C014384	IND FERITE BEAD AX
U62,63,67,68	C014386-05	CONN SKT DIP 20P
U44	C014386-11	IC SOCKET 24P PC5
U10	C025988	IC PC900 DIP 6P
	C025993-001	CRYSTAL 2.4576 MHZ
D1,2,3,8,10,11	C060607	DIODE SILICON(SWITCHING)
R178,217	C060629	RES JMPR 0 AX
R178,217	C070033	CONN DIN 5P MIDI RIGHT ANGLE
J1	C070119	SW PUSH SPJ312U
J13	C070129	CONN 40P RIGHT ANGLE
J4	C070133-002	CONN D 25P FEMALE RT-ANGLE
J18	C070446-002	CONN SIP 10P
U3,27	C070447	IC TL497A DIP 14P
P7,9,10,11	C070448	RES NET SIP 10K 9P
C96	C070450-008	CAP ELEC 470UF 35V 20% AX
C2,6,11,67	C070450-101	CAP ELEC 4.7UF 25V 20% AX 18MM
L45	C070471-002	IND 220UH 10% AX
C1	C070499-001	CAP ELEC 22UF 16V +-20% AX
C29,110	C070499-004	CAP ELEC 100UF 16V 20% AX
	C070512-003	NUT M3
P4	C070567-006	RES NET 1K*8 9P
	C070571-004	SCREW, PHIL FLAT HD,M3X 12MML
U8	C070734-003	IC LM7809 TO-92 3P
P1,2,3	C070737-005	RES NET 220/330 8P
W10,800	C070761	CONN SKT SHUNT SHORT TYPE
J12	C100013-001	CONN HEADER SINGLE 2PIN STR
W10	C100307-001	CONN HEADER SIP 1X3
P12	C101008-122	RES NET SIP 1.2K 9P
P5,8,13, 14,15,16,17	C101008-472	RES NET SIP 4.7K 9P
R112,126	C101013-100	RES CHIP 10 1/10W 5%
R109,118,144, 146,152,156, 157,R163,169, 174,175,208, 213,215,R228, 243,248,82	C101013-102	RES CHIP 1K OHM 1/10W 5%

ITEM	PART NUMBER	DESCRIPTION
R2,5,34, 44,55,58, 84,110,111 R119,120,121, 122,123,124, 130,R131,134, 153,177,182, 185,188,R193, 201,204,205, 206	C101013-103	RES CHIP 10K 1/10W 5%
R56,59,66, 68,87,90	C101013-104	RES CHIP 100K 1/10W 5%
R189,191,195,197	C101013-105	RES CHIP 1M 1/10W 5%
R7,73	C101013-122	RES CHIP 1.2K 1/10W 5%
R3,6	C101013-123	RES CHIP 12K OHM 1/10W 5%
R241	C101013-220	RES CHIP,221/10W 5%
R57,86,92,207	C101013-222	RES CHIP 2.2K OHM 1/10W 5%
R39,50,162, 168,212,216, 219,220,R221, 222,223,229, 230,233,236, R237,238,239	C101013-330	RES CHIP 33 1/10W 5%
R29,148	C101013-332	RES CHIP 3.3K OHM 1/10W 5%
R67,88	C101013-333	RES CHIP 33K 1/10W 5%
R43,114	C101013-392	RES CHIP 3.9K 1/10W 5%
R176	C101013-393	RES CHIP 39K 1/10W 5%
R190,192,196,198	C101013-471	RES CHIP 470 1/10W 5%
R16,17,38, 40,42,71, 72,81,89 R147,159,160, 161,166,167, 173,R180,181, 184,194,199, 200,209,R214, 218,231,232	C101013-472	RES CHIP 4.7K 1/10W 5%
R69,94,128,129	C101013-473	RES CHIP 47K 1/10W 5%
R125,132	C101013-513	RES CHIP 51K OHM 1/10W 5%
R75-78,115, 136-143,149-151	C101013-560	RES CHIP 56 1/10W 5%
R49,60-64, R95-103,127, 165,183,R186, 187,202,203,211, 224,225,R226,227, 235	C101013-680	RES CHIP 68 1/10W 5%
R155	C101013-912	RES CHIP 9.1K OHM 1/10W 5%
R25,27,51,91	C101021-101	RES 100 5%1/4W 200PPM SMD
R133,145,154	C101021-151	RES 150 5%1/4W 200PPM SMD

ITEM	PART NUMBER	DESCRIPTION
R93	C101021-200	RES CHIP,20 1/4W 5%
R234	C101021-220	RES CHIP,22 1/4W 5%
R1,4,18,19, 41,113,158,210, 242,R249,250	C101021-221	RES CHIP,220 1/4W 5%
R10-15,20-24, 26,28,35,9	C101021-270	RES 27 5% 1/4W 200PPM SMD
R164,170,171,172	C101021-470	RES 47 5% 1/4W 200PPM SMD
R36,37,48,52, 53,54,65,83,85	C101021-750	RES CHIP,75 1/4W5%
C147	C101205-472	CAP ELEC 4700UF 16V AX
C181,48	C101212-010	CAP ELEC 1UF 50V 20% AX
C88,91,141	C101212-100	CAP ELEC 10UF 50V 20% AX
C78	C101212-2R2	CAP ELEC 2.2UF 50V 20% AX
C92,127	C101212-3R3	CAP ELEC 3.3UF 50V 20% AX
C198,202,208, 212,217,246,247	C101219-100	CAP CER CHIP 10PF 50V 5%
C21,27,28, 31,32,33,58,59,81	C101219-101	CAP CERA CHIP 100PF 50V 5%
C8	C101219-151	CAP CER 150PF 5% 50V SMD
C12-18	C101219-221	CAP CERA CHIP,220PF 50V 5%
C66	C101219-271	CAP CER CHIP 270PF 50V 5%
C106,107,145	C101219-300	CAP CERA CHIP 30PF 50V 5%
C9	C101219-331	CAP CERA CHIP 330PF 50V 5%
C19,20,25	C101219-470	CAP CER 47PF 5% 50V SMD
C113,114,116, 187,200,214, 216,C240,63	C101219-680	CAP CER CHIP 68PF 50V 5%
C125,126,168, 170,188,190	C101219-681	CAP CER CHIP 680PF 50V 5%
C89	C101220-821	CAP CER CHIP 820PF 50V10%
C3,169,171, 189,191	C101221-103	CAP CERA CHIP .01UF 50V +80-20
C41,45,46, 74,102,103, 105,136,C137, 142,150,152, 156,158,165, C172,173,175, 180,185,194, 195,C196,206, 213,215,225, 227,230,C241, 243,248,117	C101221-223	CAP CERA CHIP .022UF50V+80-20
C85,86,90,95	C101221-333	CAP CERA CHIP .033UF50V+80-20
C232	C101221-473	CAP CERACHIP 0.047UF50V+80-20%

ITEM	PART NUMBER	DESCRIPTION
L1-4,6-26, 28,31,44, 55,79,81, 83,L86-96, 100,101,103, 106,107,108, L113-116	C101403-102	FILTER NOISE 1000PF
L59	C101411-680	IND 68UH 10% AX SHT BOD
F1,2	C101814	FUSE MICRO 5A 125V AX
J20,21	C101901-005	CONN HEADER DOUB.ROW 30P(15*2)
J16,17	C101901-008	CONN HEADER 2 * 25P
J7,8	C101990-001	CONN EARPHON JACKSTERDBLSWITCH
U22,23	C103803-001	IC LM386 AUDIO AMP SOP
U1	C104522-001	IC LM555 TIMER (SOP)
J2	C300269-001	CONN D SUB MALE RT-ANGLE 9P
U20	C302096-001	IC CUSTOM AJAX FDD CNTRL 28PDP
P6	C302387-044	CONN 44P 2X22 2MM STRAIGHT
U42,43,59,60,61	C302624-244	IC 74HC244 SOIC 20P
U17	C302799-002	IC YM3439-F 44P PQFP
J9	C302821-001	CONN DSUD 26P 3ROW FEMALE
J6	C302822-001	CONN SCSI-II 50P FEMALE
J6	C302823-001	CONN DSUB 19P MALE
U30	C302824-001	IC STV8438 PQFP 44P
U34	C302829-001	IC CUSTOM VIDEL 120P QFP
U67	C302830-001	IC GAL16V8-12 DIP 20P ECLK
U62	C302831-001	IC GAL16V8-12 DIP 20P UDS/LDS
U63	C302832-001	IC GAL 16V8-12 DIP 20P DSACK
U68	C302833-001	IC GAL16V8-12 DIP 20P AS/BG
U44	C302834-001	IC GAL20V8-12 DIP 24P DSP
U26	C302889-008	IC 74LS08 SOIC 14P
U66	C302889-373	IC 74LS373 SOIC 20P
U25	C302892-004	IC 74HCT04 SOIC 14P
U2,11,35,54	C302893-006	IC,7406,14P SOIC
U7	C302897-001	IC 53C80 PLCC 44P
U9	C302900-001	IC LM387 DIP 8P
J22	C302883	FAN 12V 40*40*10MM

ITEM	PART NUMBER	DESCRIPTION
C4,5,10, 30,34,35, 38,39,42, 43,C44,47, 52,53,64, 65,68,76, 77,C80,82, 97,99,100, 101,104,108, C109,111,112, 115,118,119, 120,C123,130, 132,134,135, 143,144,C146, 148,149,151, 153,154,155, C157,159-164, 166,167,174, 23,C176-179, 182,183,184, 186,192,C193, 197,199,201, 203,204,205, C207,209,210, 211,218,219, 22,98	C302904-104	CAP CERA CHIP,0.1UF 50V+80-20%
C223	C302904-474	CAP CER CHIP .47UF 50V +80-20
U28,51	C302967-001	CONN SKT 44P PLCC SMT
U33	C302967-003	CONN SKT 68P PLCC SMT
C7	C302985-001	CAP ELEC 0.1UF 50V 20% AX
U56	C302995-001	IC CUSTOM COMBEL 208P QFP
U36	C302996-001	IC CUSTOM SDMA 144P QFP
U16	C302997-001	IC 3486 16P SOIC
U49,50	C302998-001	IC 556 14P SOIC
U51	C302999-001	IC EPROM 4M 44P PLCC
U55	C303001-001	IC 68LC030 132P QFP
U38	C303002-001	IC DSP56K 80P QFP
U28	C303003-001	IC STEREO AUDIO CODEC 44P PLCC
U45,48,53	C303004-001	IC 32KX8 SCRAM 28P SOJ
J14	C303005-008	CONN HEADER 8P STRAIGHT
C40,55	C303013-154	CAP CERA CHIP 0.15UF 25V 10%
C122,128,131, 133,139,26, 79,94	C303013-474	CAP CERA CHIP 0.47UF 25V 10%
C124,129,140	C303020-103	CAP CERA CHIP .01UF50V
C121,57	C303021-227	CAP ELEC 22OUF 16V 20% AX
C138,54,56,83,84	C303021-476	CAP ELEC 47UF 16V 20% AX
U12	C303023-001	OSC 3.672MHZ 8P W/DIS
U41	C303023-002	OSC 25.175MHZ 8P W/DIS
U37	C303023-003	OSC 32MHZ 8P W/DIS
D9	C303029-001	DIODE FAST REC 1N4935

ITEM	PART NUMBER	DESCRIPTION
U21	C303030-001	IC LF347 14P SOIC
U5	C398016-001	IC 1488 RS-232 DRIVER 14P SOIC
U14,6	C398017-002	IC 1489A RS-232 REC 14P SOIC
J19,23	C398064-002	CONN D SUB 15P 3 ROW FEMALE
J3	C398087-001	CONN MINI DIN 8P
U31	C398106-001	IC MC68901 PLCC 52P
U13	C398109-001	IC Z85C30 10MHZ 44P PLCC
U15	C398112-030	IC 26LS30 DIP 16P
U19	C398112-031	IC 26LS31 DIP 16P
U64	C398170-001	IC DS1287 DIP 24P .600
U40	C398173-074	IC 74ACT7414P SOIC
U39	C398173-157	IC 74ACT157 16P SOIC
U24,52	C398784-001	IC 68B50 ACIA 24P
U32	CA070024	ASSY CABLE FLAT 34P
J15	CA07023-009	CONN FDDPWR CABLE 4P 280MM

MECHANICAL ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
	C070004-004	SCREW SELF TAP PAN HD 3*10
	C070004-015	SCREW SELF TAP M3*7L
230	C070012	RUBBER FOOT
	C070200-001	SCREW PAN HEAD M3*5
	C070200-003	SCREW PAN HEAD M3X8
	C070322-003	COLLAR A BLACK 18.5MM ST
	C070323-003	COLLAR B
40	C302769	SHIELD TOP FALCON030
10	C302770	SHIELD BOTTOM FALCON030
20	C302771	PCB INSULATOR FALCON030
70	C302774-001	COVER BTM FALCON030 NTSC
60	C302779	SHIELD I/O PLATE FALCON030
160	C302780	SHIELD COVER FALCON030
170	C302781	INSULATOR SPEAKER FALCON030
190	C302782	RETAINER, SPKR FALCON030
	C303075-001	SCREW PPH 6-32x1"
10	CA401280-001	ASSY TOP COVER FALCON030
180	CA401337-001	ASSY SPKR FALCON030
	C302775	BRACKET FAN MOUNTING FX-1

SECTION EIGHT
GLOSSARY

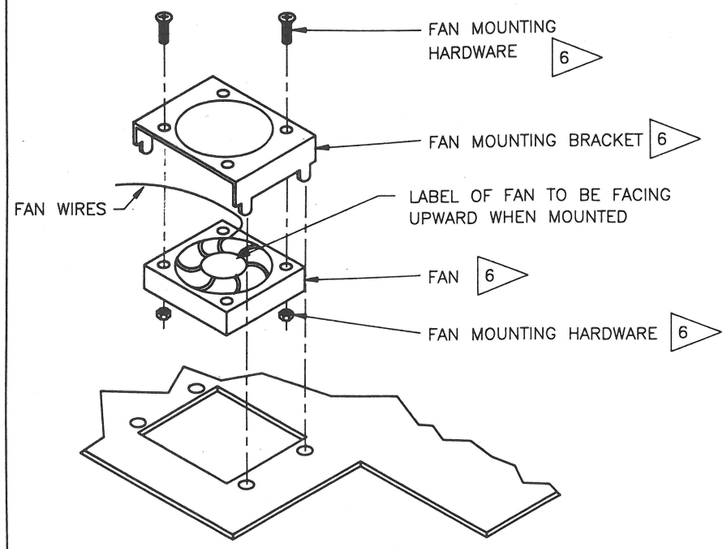
AJAX IC	Floppy Disk Controller.
6850	Also ACIA (Asynchronous Communication Interface Adapter). Each one provides an asynchronous communications channel. In the FALCON030, there are two 6850s, one for keyboard communication, and one for MIDI communication.
68901	See MFP.
BUS ERROR	COMBEL IC has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller in the COMBEL IC fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.
CPU	The 68030 microprocessor.
DMA	Direct Memory Access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, and takes place independent of the CPU, so that the CPU can be processing while DMA is taking place. The COMBEL IC arbitrates the bus between the CPU and DMA.
DMA CONTROLLER	Atari proprietary SDMA chip which controls the DMA process. All disk I/O goes through this device.
EXCEPTION	A state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also System Errors, or a 68030 reference for more detail.
COMBEL	Atari proprietary chip which ties together all system timing and control signals. It provides ROM/RAM/IO address decode, Register decode (only for registers that remain in the COMBEL), Interrupt priority encoding and IACK logic, Paddle circuit, Joystick circuit, Clock dividers, Video registers (with modifications to support up to 14MB DRAM memory space), and the Blitter.

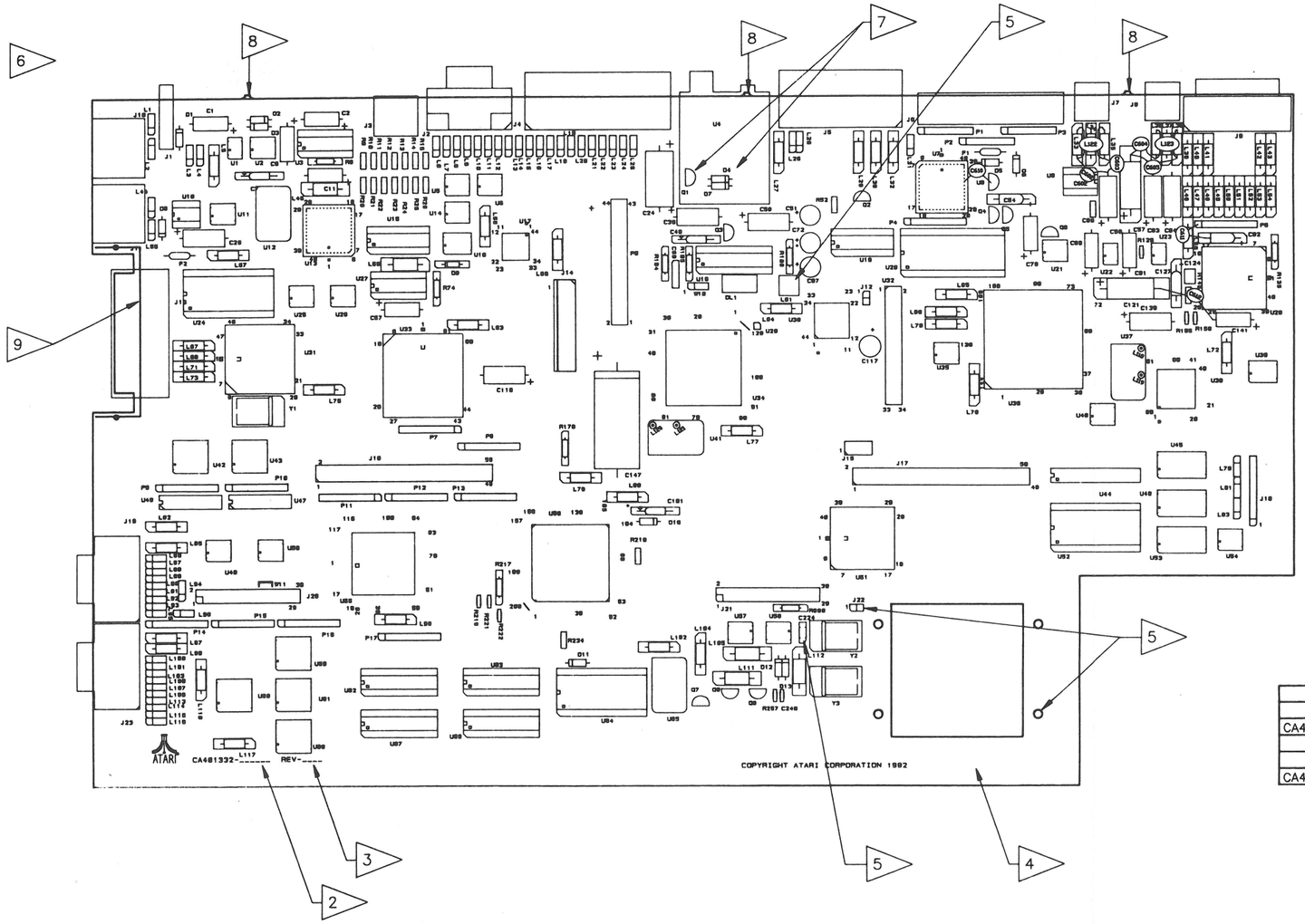
HALT	State in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bidirectional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.
HSYNC	Timing signal for the video display. Determines when horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) It is also encoded onto IPL2..0 to cause a level 2 auto-vectored interrupt to the CPU.
INTERRUPT	A request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: The highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and COMBEL.
MIDI	Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the FALCON030, consists of a 6850 communication chip, driver and receiver chips (74LS04, 74LS05, and PC-900 optoisolator), and an MFP interrupt channel.
MFP	Multi-Function Peripheral, aka 68901. Interrupt control and timers.
SCC	Serial Communications Controller, contains USART for RS232 communication and LAN interface. See Theory of Operation, Main System.
MODULATOR	Device which modulates a composite video signal, combined with audio, onto an RF carrier for output to a television.
PHASE LOCKED LOOP	Circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen.
PSG	Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.

RS232C	Electrical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the FALCON030 computers, consists of the MFP, PSG, 1488, and 1489 chips.
SUPERVISOR MODE	State of the CPU in which it is allowed to access all hardware and RAM locations, and perform some privileged instructions. Determined by the state of a bit in the Status Register.
USER MODE	State of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.
VSYNC	Signal used for vertical synchronization of CRT display device.
YM2149	See PSG.

SECTION NINE
SCHEMATICS AND PCB LAYOUT

REV	REVISION DESCRIPTION	DATE	APPROVED
A	REL TO PROD PER ECO 1505	--	--
B	REVISED PER ECO 1600	1/26/93	J. SMITH
C	REVISED PER ECO 1604	3/16/93	J. SMITH
D	REVISED PER ECO 1613	3/16/93	J. SMITH
E	REVISED PER ECO 1621	3/2/93	J. SMITH
F	REVISED PER ECO 1625	4/30/93	J. SMITH
G	REVISED PER ECO 1642	6/4/93	
H	REVISED PER ECO 1643	6/4/93	
J	REVISED PER ECO 1641	6/4/93	





11. JUMPER R221 OR REPLACE WITH Ø OHM RESISTOR. C208 NOT INSTALLED.

10. TURN SCREW OF L61 TO THE FULL CLOCKWISE POSITION.

9 > INSTALL CONNECTOR SHIELD FOR J13, ATARI P/N C070335-001.

8 > EXCESS MATERIAL FROM BREAKAWAY TABS MUST BE REMOVED FROM BACK EDGE OF PCB.

7 > APPLY INSULATING TAPE OVER Q1, D4, AND D7 WHEN RF MODULATOR U4 IS INSTALLED.

6 > SEE BOM CA401335 FOR PART NUMBERS.

5 > MASK THE FOUR (4) FAN MOUNTING BRACKET HOLES AND THE PLATED THRU HOLES OF L61, C224, AND J22 BEFORE SOLDERING.

4 > SERIALIZE PCB AS SHOWN BELOW:

XX XX 2 X XXXXXX

- FACTORY CODE — REFER TO ATARI DWG #C070138
- YEAR/MONTH — LAST FIGURE OF A.D.; 1 THROUGH C: 1 = JANUARY, C = DECEMBER
- CONTROL CODE
- VERSION: 1 = NTSC, 2 = PAL I, 3 = PAL B, 4 = PERITEL
- SEQUENTIAL NUMBER STARTING AT 000001

CONTROL CODE	DESCRIPTION
0	PILOT PRODUCTION
1	NOT USED
3	REWORK FOR FCC/REMOVE AUDIO BASS BOOST

3 > MARK CURRENT REVISION OF ASSEMBLY. USING WHITE EPOXY INK.

2 > MARK VERSION NUMBER USING WHITE EPOXY INK. REFER TO VERSION CHART.

1. SEE SEPARATE PARTS LIST.

NOTES: (UNLESS OTHERWISE SPECIFIED)

VERSION CHART		
P/N	COUNTRY	REV
CA401332-001	US-CAN	J
-002	GERMANY	H
-003	UK	H
CA401332-004	FRANCE	A

CA401381-TAB	FALCON030
CA401379-TAB	FALCON030
NEXT ASSY	USED ON ORIGINAL MODEL
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES
ON LINEAR DIMENSIONS: UNDER 30 ±; 30 THRU 300 ±; OVER 300 ±
ON ANGULAR DIMENSIONS ±

MATERIAL: NONE
FINISH: NONE

		DATE
DRAWN BY	BELAND	6/25/92
CHECKED		
ENGINEER	J. SMITH	2/25/92
APPROVED	ULASZEK	2/25/92
APPROVED AT	R.J. Henderson	6-8-93

ATARI CORPORATION

TITLE: PCB SUB ASSY, FALCON030

SIZE	DRAWING NO.	REV
D	CA401332-TAB	J

SCALE NONE — SHEET 1 OF 2

REV	REVISION DESCRIPTION	DATE	APPROVED

ACTION REQUIRED	REF	ECO#
THE FOLLOWING REWORK SHOULD BE APPLIED TO ALL REVISION 2 FAB PCB'S C303006-001. COMPONENT SIDE: LIFT COMPONENT LEAD U55 PIN 7 FROM PCB LIFT COMPONENT LEAD U67 PIN 19 FROM PCB. ADD JUMPER FROM LIFTED COMPONENT LEAD U55 PIN 7 TO LIFTED COMPONENT LEAD U67 PIN 19 SOLDER SIDE: ADD JUMPER WIRE FROM SOLDER PAD U67 PIN 15 TO U67 PIN 19.	U55 U67	1488

PAL COLOR BURST FREQ SYNCHRONIZED WITH HSYNC

ACTION REQUIRED	REF	ECO#
THE FOLLOWING REWORK SHOULD BE APPLIED TO ALL REVISION 2 FAB PCB'S C303006-001. LIFT COMPONENT LEAD U58 PIN 2 FROM PCB ADD A 2K RESISTOR R600 IN SERIES BETWEEN LIFTED COMPONENT LEADS U58 PIN 2 AND Y2 PIN 2.	U58 R600 Y2	1498

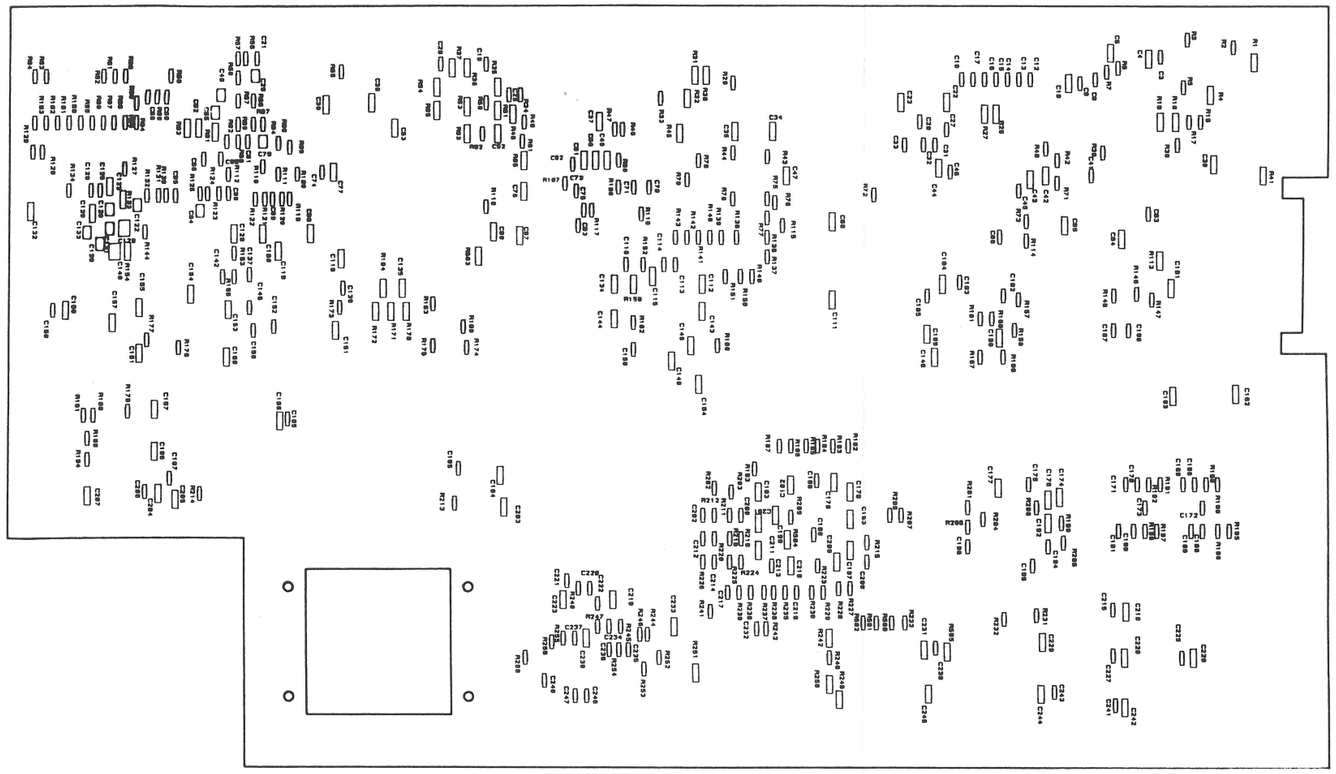
ACTION REQUIRED	REF	ECO#
THE FOLLOWING REWORK SHOULD BE APPLIED TO ALL REVISION A AND BELOW FAB PCB's C303006-001. LIFT COMPONENT LEAD U4 PIN 1 FROM PCB. ADD A 10 OHM RESISTOR R601 IN SERIES BETWEEN LIFTED COMPONENT LEAD U4 PIN 1 AND SOLDER PAD U4 PIN 1. ADD A 10UF CAPACITOR C601 FROM LIFTED COMPONENT LEAD U4 PIN 1 AND THE NEGATIVE TERMINAL OF C48 (GND).	U4 R601 C601	1600

ACTION REQUIRED	ECO#
THE FOLLOWING MODIFICATIONS SHOULD BE APPLIED TO REVISION A FAB PCBS: 1. INSTALL L122 (PN 500054) IN LOCATION L33 AND L35. DO NOT INSTALL PN C014384 IN THESE LOCATIONS. 2. INSTALL L123 (PN 500054) IN LOCATION L36 AND L38. DO NOT INSTALL PN C014384 IN THESE LOCATIONS. 3. INSTALL ZERO OHM JUMPER (PN C060629) IN LOCATION L34 AND L37. DO NOT INSTALL PN C014384 IN THESE LOCATIONS. 4. ADD C602 (PN C070535-008) ON COMPONENT SIDE FROM LOCATION L33 PIN 2 (ROUND PAD) TO C56 PIN 2 (NEGATIVE LEAD). 5. ADD C603 (PN C070535-008) ON COMPONENT SIDE FROM LOCATION L35 PIN 1 (SQUARE PAD) TO C56 PIN 2 (NEGATIVE LEAD). 6. ADD C604 (PN C070535-008) ON COMPONENT SIDE FROM LOCATION L36 PIN 1 (SQUARE PAD) TO C57 PIN 2 (NEGATIVE LEAD). 7. ADD C605 (PN C070535-008) ON COMPONENT SIDE FROM LOCATION L38 PIN 1 (SQUARE PAD) TO C57 PIN 2 (NEGATIVE LEAD). 8. ADD C606 (PN C070535-008) ON SOLDER SIDE FROM LOCATION L33 PIN 1 (SQUARE PAD) TO J7 PIN 1 (GND). 9. ADD C607 (PN C070535-008) ON SOLDER SIDE FROM LOCATION L35 PIN 2 (ROUND PAD) TO J7 PIN 1 (GND). 10. ADD C608 (PN C070535-008) ON SOLDER SIDE FROM LOCATION L36 PIN 2 (ROUND PAD) TO J8 PIN 1 (GND). 11. ADD C609 (PN C070535-008) ON SOLDER SIDE FROM LOCATION L38 PIN 2 (ROUND PAD) TO J8 PIN 1 (GND). 12. ADD C610 (PN C070535-016) ON COMPONENT SIDE FROM U7 PIN 36 TO U8 PIN 2 (CENTER PIN). 13. ADD C611 (PN C070535-016) ON COMPONENT SIDE FROM P5 PIN 1 TO C92 PIN 2 (ROUND PAD, NEGATIVE LEAD). 14. ADD C612 (PN 070535-016) ON COMPONENT SIDE FROM C121 PIN 2 (ROUND PAD, NEGATIVE LEAD) TO C141 PIN 2 (ROUND PAD, NEGATIVE LEAD). 15. INSTALL PIN 8 OF U37, WHEN U37 IS HALF SIZE (OR PIN 14 IF U37 IS FULL SIZE), THROUGH L118 (PN 500059). 16. INSTALL PIN 5 OF U37, WHEN U37 IS HALF SIZE (OR PIN 8 IF U37 IS FULL SIZE), THROUGH L119 (PN 500049). 17. INSTALL PIN 8 OF U41, WHEN U41 IS HALF SIZE (OR PIN 14 IF U41 IS FULL SIZE), THROUGH L120 (PN 500049). 18. INSTALL PIN 5 OF U41, WHEN U41 IS HALF SIZE (OR PIN 8 IF U41 IS FULL SIZE), THROUGH L121 (PN 500049).	1604

ACTION REQUIRED (CONTINUED)	ECO#
19. SOLDER ONE END OF W1 (PN 500060) TO J7 PIN 1 (GROUND) AND TO LOGIC GROUND TRACE AT EDGE OF PCBA. W1 SHOULD BE CUT TO 1 INCH LENGTH WITH APPROXIMATELY 13/16 INCHES EXTENDING BEYOND EDGE OF PCBA. THE OTHER END WILL BE SOLDERED TO THE CHASSIS. 20. SOLDER ON END OF W2 (PN 500050) TO J8 PIN 1 (GROUND) AND TO LOGIC GROUND TRACE AT EDGES OF PCBA. W2 SHOULD BE CUT TO 1 INCH LENGTH WITH APPROXIMATELY 13/16 INCHES EXTENDING BEYOND EDGE OF PCBA. THE OTHER END WILL BE SOLDERED TO THE CHASSIS.	1604

ACTION REQUIRED	ECO#
THE FOLLOWING MODIFICATIONS SHOULD BE APPLIED TO REV H: 11. JUMPER R221 OR REPLACE WITH 0 OHM RESISTOR C208 NOT INSTALLED.	1643

ACTION REQUIRED	ECO#
THE FOLLOWING MODIFICATIONS SHOULD BE APPLIED TO REV J: -THE FOLLOWING COMPONENTS ARE NOT TO BE INSTALLED: R56, R57, R90, R92. -INSTALL C613 (101219-561 SOLDERED IN PARALLEL WITH R131 ON SOLDER SIDE. -INSTALL C614 (C101219-561) SOLDERED IN PARALLEL WITH R124 ON SOLDER SIDE. -INSTALL C615 (C101219-561) SOLDERED IN PARALLEL WITH R66 ON SOLDER SIDE. -INSTALL C616 (C101219-561) SOLDERED IN PARALLEL WITH R67 ON SOLDER SIDE. -INSTALL C617 (C101219-561) SOLDERED IN PARALLEL WITH R87 ON SOLDER SIDE. -INSTALL C618 (C101219-561) SOLDERED IN PARALLEL WITH R688 ON SOLDER SIDE. -INSTALL 1K OHM RESISTOR (C101013-102 IN LOCATION C90 & C91. -INSTALL R602 (14-5103) FROM U21 PIN 2 TO U21 PIN 11 ON COMPONENT SIDE	1641



SILKSCREEN
SOLDER SIDE

ATARI CORPORATION

TITLE	PCB SUB ASSY, FALCON030	
SIZE D	DRAWING NO. CA401332-TAB	REV J
SCALE NONE	SHEET 2 OF 2	

REV	REVISIONS DESCRIPTION	DATE	APPROVED
1	INITIAL RELEASE	1/6/93	
A	ENGINEERING RELEASE	3/1/93	
B	PRODUCTION RELEASE ECO 1644	5/13/93	

		DRAWN BY TRH DATE	ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089
		CHECKED DATE	
CA401273-XXX		ENGINEER DATE 7/1/93	TITLE FALCON 030 SCHEMATIC
NEXT ASSEMBLY	USED ON ORIGINAL MODEL	APPROVED DATE	SIZE D / CODE / NUMBER 500047-001 / REV B
APPLICATION		APPROVED DATE 7-1-93	SHEET 1 OF 14

CCLK

STUFFED IN PAL SYSTEMS ONLY

12V

HSYNC

(SEE L77)

VIDEL25M

25M

STUFFED IN NON-PAL SYSTEMS ONLY

32.084988MHZ

IN PARENTHESIS, VALUE FOR NTSC
NON PARENTHESIS - PERITAL

(VALUE=32.215905MHz)

FUSE

POWER

FAN

XRESET
XBERR
XHALT
XBR
XBGK
XDTACK
XAS
XLDS
XUDS
RXW
XVPA
XVMA
FC0
FC1
FC2

1.2KX8

XROM3
XROM4
XUDS
XLDS

XROM2

ADDR[23:0]

DATA[15:0]

40PCART

J13

ATARI CORP.		
1196 BORREGAS AVE.		
SUNNYVALE, CA. 94089		
TITLE: FALCON 030 SCHEMATIC		
SIZE: D	CODE:	NUMBER: 500047-001 REV: B
SHEET 2 OF 14		

* – OPTIONAL COMPONENTS

QC 33 A233 ECLK

C63 68PF C187 68PF

RES J1 PULSER

R2 10K U2 KHZ500

R5 10K D1 1N914 C7 1UF

LM555 U1 C3 10NF C1 22UF

12K R3 XRESET

XHALT

R16 4.7K

R4 220 R18 * R1 * R19 *

J10 MIDI OUT

FB

PC900 U10

R41 220 D8 1N914 J11 MIDI IN

R17 4.7K U11 74LS06

R38 4.7K

C76 0.1UF

N6850

R113 220 ECLK RXW

MC6850 U24

IRQ TXC RXC TXD RXD RTS CTB DCD

ADDR2 ADDR1 RS RXW

DATA15 DATA14 DATA13 DATA12 DATA11 DATA10 DATA9 DATA8

RTCCS RTCAS RTCDS RXW

C1287 U64

STBY POWER CKFS PS RST IRQ SQW CKD X2 X1 MOT GND

AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0

R243 1K D11 1N914 C232 47NF

R191 4.7K R147 4.7K R214 4.7K

KHZ500W U26

KTOK

MC6850 U52

R168 10K TXD

AUDIOS R144 1K AGND C174 1UF IDERST XSPKON

YM-3439 PSG U17

CLK2 SNDIR SNDCS

IOA7 IOA6 IOA5 IOA4 IOA3 IOA2 IOA1 IOA0 DOSEL SOSEL

DATA15 DATA14 DATA13 DATA12 DATA11 DATA10 DATA9 DATA8

IOB7 IOB6 IOB5 IOB4 IOB3 IOB2 IOB1 IOB0 PSG7 PSG6 PSG5 PSG4 PSG3 PSG2 PSG1 PSG0

PSG [7: 0]

U25 74HCT04 XDSPRESET

SOUNDINT

CLK4

MC68901 U31

XTAL1 XTAL2 2.4576MHZ BCLK4 Y1 C107 30PF C106 30PF R149 3.3K

TAI TBI TAO TBO TCO TDO SI SO RC TC

DE SNDINT

XMFPCS XLDS EDTACK XRESET XMFPINT XIACK

R184 4.7K

DSPINT

DATA [15: 0]

ADDR [23: 0]

XIEO_MFP XIEI_MFP

IDEIRQ XDISKINT U25 U26 74HCT04

R146 1K

C65 C207 C101 C135 C219 C34 C115 C64 C149 0.1UF

U54 U25 74HCT04

U54 U2

U6 1489 RI C33 100PF

T FILTERS

DB-25P PARALLEL PORT

DOSEL U26 U25 74HCT04 U54 IDE_ACT

R194 4.7K R161 4.7K J18 KEYBOARD

XRESET KTOK KROK

PRTACK

R29 3.3K SELECT_IN

J4

ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE: FALCON 030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: 500047-001	REV: B
			SHEET 3 OF 14

FOR NON MODULATOR SYSTEMS ONLY

HSYNC
VSYNC
1N914
2N3904
AVGND
CSYNC
COLOR
CCLK
ESYNC
REMOVE FOR PAL
MC1377
U18
AUDIO
DL1
12V
VCC
GND
STMOD
U4

VER_INT
WDATV
RDATV
HINTC
VREQC
RAMHV

* - REQUIRES VALUE CHANGE FOR PAL

FOR MODULATOR SYSTEMS ONLY

NOTE: JMP2_ST MUST BE PLACED NEAR U35

32MHZ
CLK32
VID32MHZ

COMBEL U56

DATA [15: 0]
ADDR [23: 0]
MADDR [10: 0]
XDTACK

VIDEL U34

EXTCLK
VIDEL25M
VID32MHZ
MDATA [15: 0]
MDATA [31: 16]

SGC DAC U30

RCON
GCON
BCON
SINGLE POINT GROUND

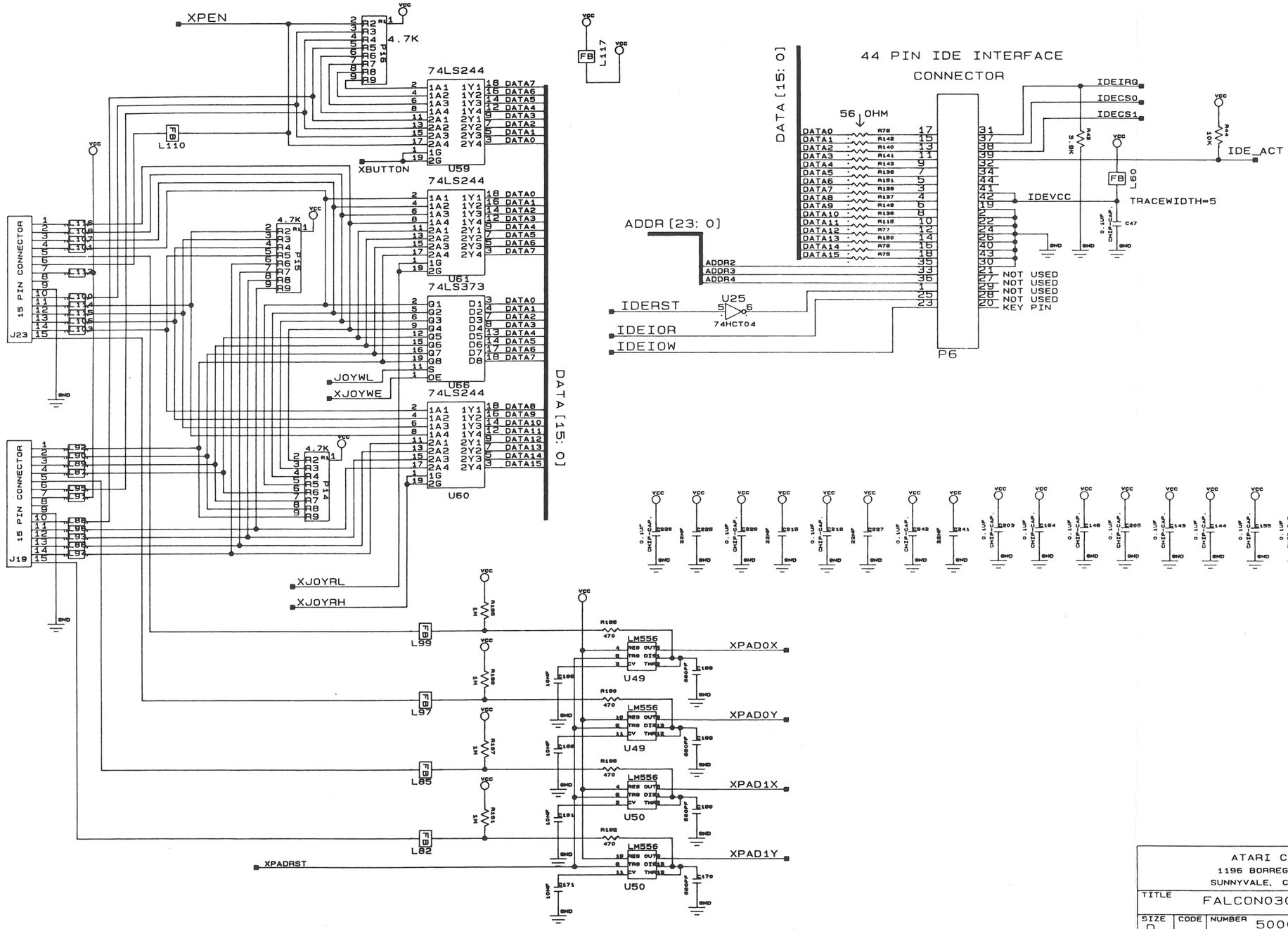
19 PIN VIDEO CONNECTOR J5

ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

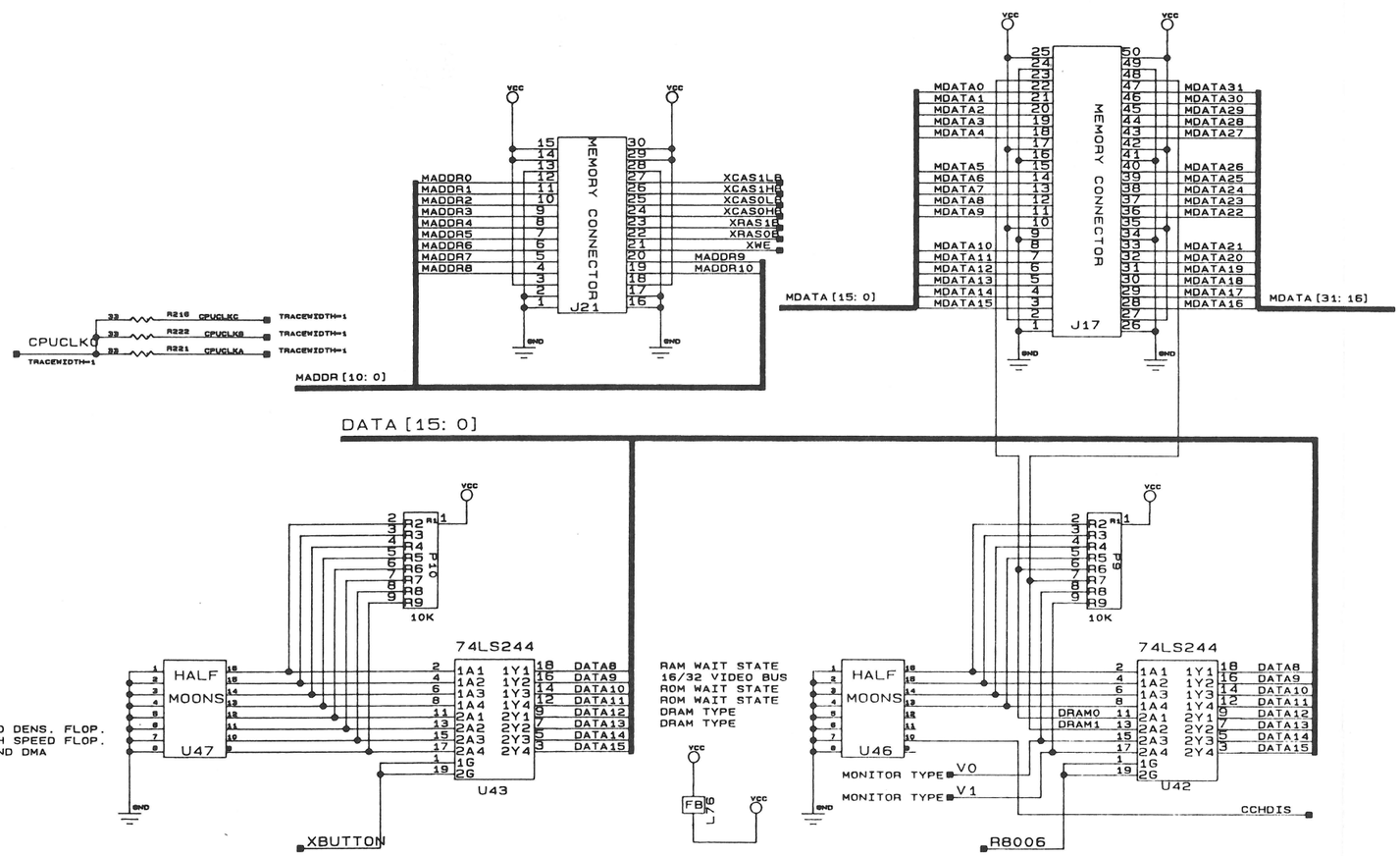
TITLE: FALCON030 SCHEMATIC

SIZE	CODE	NUMBER	REV
D		500047-001	B

SHEET 4 OF 14

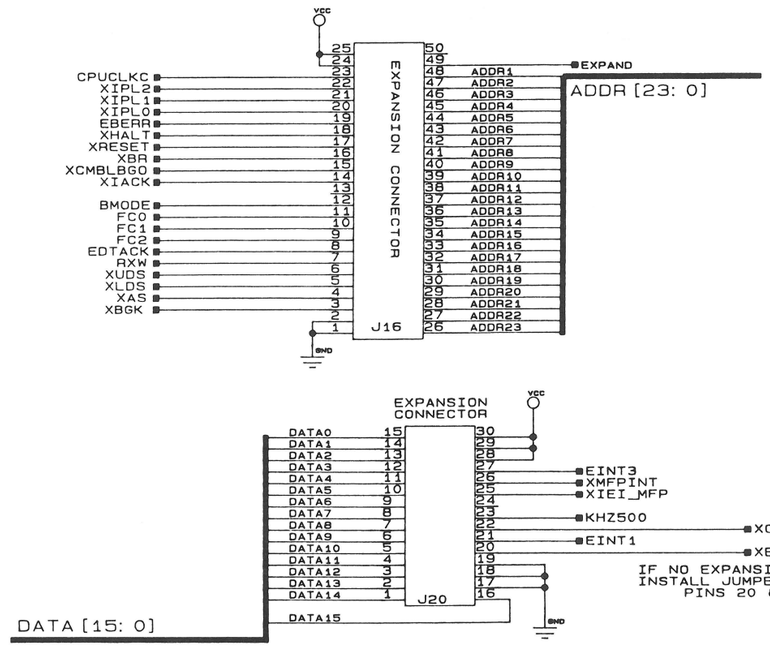


ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: 500047-001	REV: B
			SHEET 5 OF 14



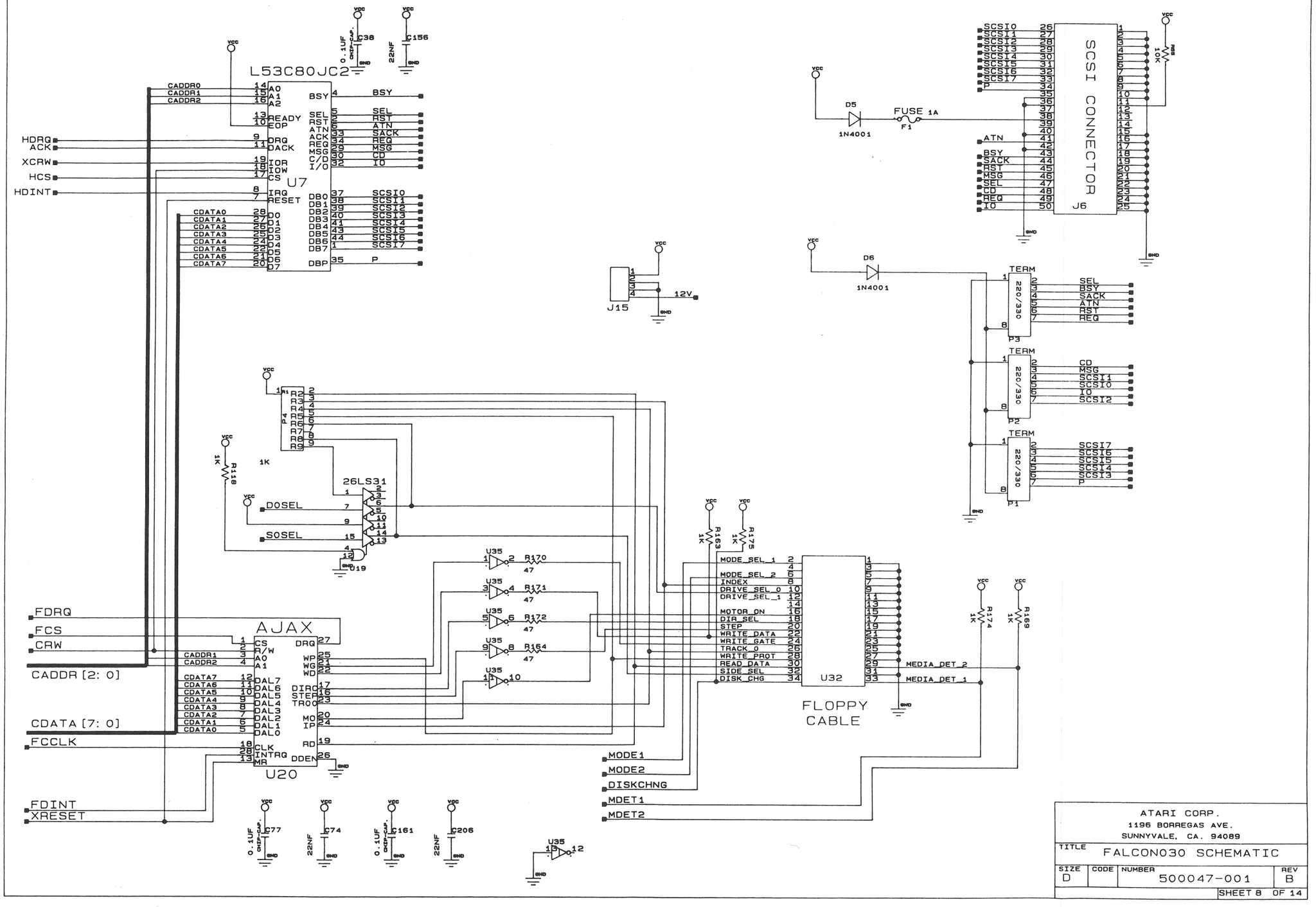
ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		500047-001	B
		SHEET 6 OF 14	



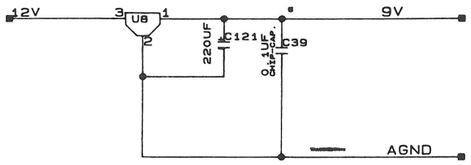
ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

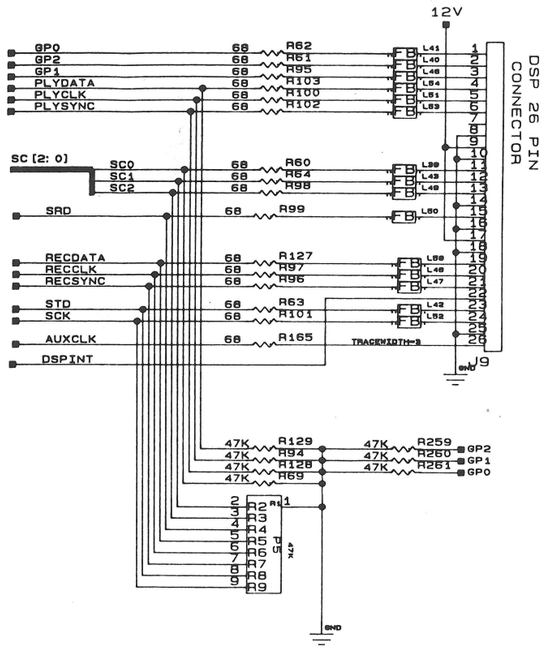
TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		500047-001	B
		SHEET 7 OF 14	



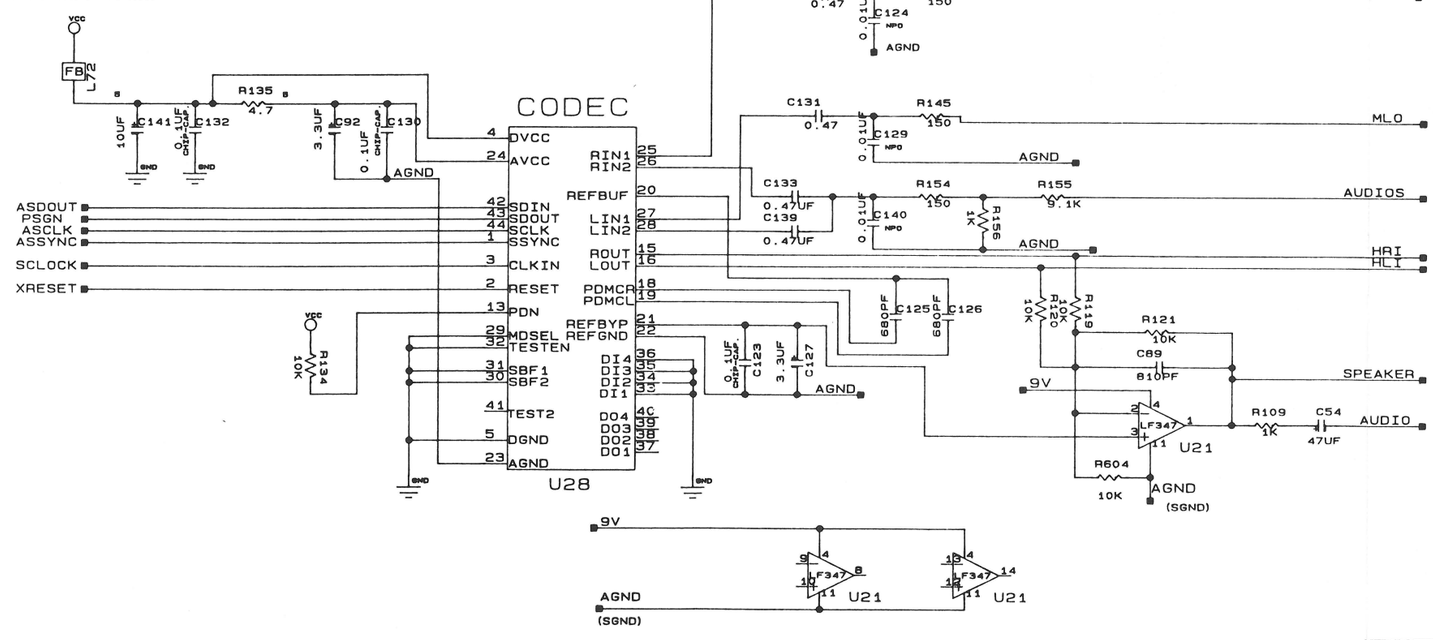
ATARI CORP.
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SUNNYVALE, CA. 94089

TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		500047-001	B
		SHEET 8 OF 14	





CLOCK TRACES, PARTICULARLY BCLOCK, SMCLK, AUXCLK MUST BE WIDE, WITH AS FEW TURNS/FEEDTHROUGHS AS POSSIBLE
USE CURVED TRACES IF POSSIBLE
KEEP TRACE WIDTHS CONSTANT, IF NOT, THEN TAPER SIGNALS TO AVOID SUDDEN IMPEDANCE CHANGES
KEEP COMPONENTS CLOSE TO THE IC'S AND LAY THEM OUT SO THAT THE SIGNAL RUNS ARE AS STRAIGHT AS POSSIBLE
USE THE CERAMIC BEAD TO BRIDGE THE ISOLATION GAP BETWEEN THE SYSTEM AND AUDIO VCC AND GND PLANES
KEEP THE DVCC AND AVCC TRACES LOW IMPEDANCE
USE WIDE TRACES AND 45 DEGREE ANGLES
USE THE ISOLATED VCC PLANE IN THIS AREA TO CARRY THE +8V POWER
AVCC IS ONLY USED BY THE CODEC



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TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		500047-001	B
		SHEET 9 OF 14	

U13 85C30

U15 26LS30

U16 DS34F86

U25 74HCT04

U5

C1488

U14 1489

U3 TL497A

U27 TL497A

J3 SCC CON.

J2 RS232 - 9 PINS

SERIAL PORT

T FILTERS

3.672MHZ

PCLK4

SYNCO

SYNC1

CLK8

ADDR[23:0]

ADDR1

BCLKA

DATA[15:0]

RI

G12V

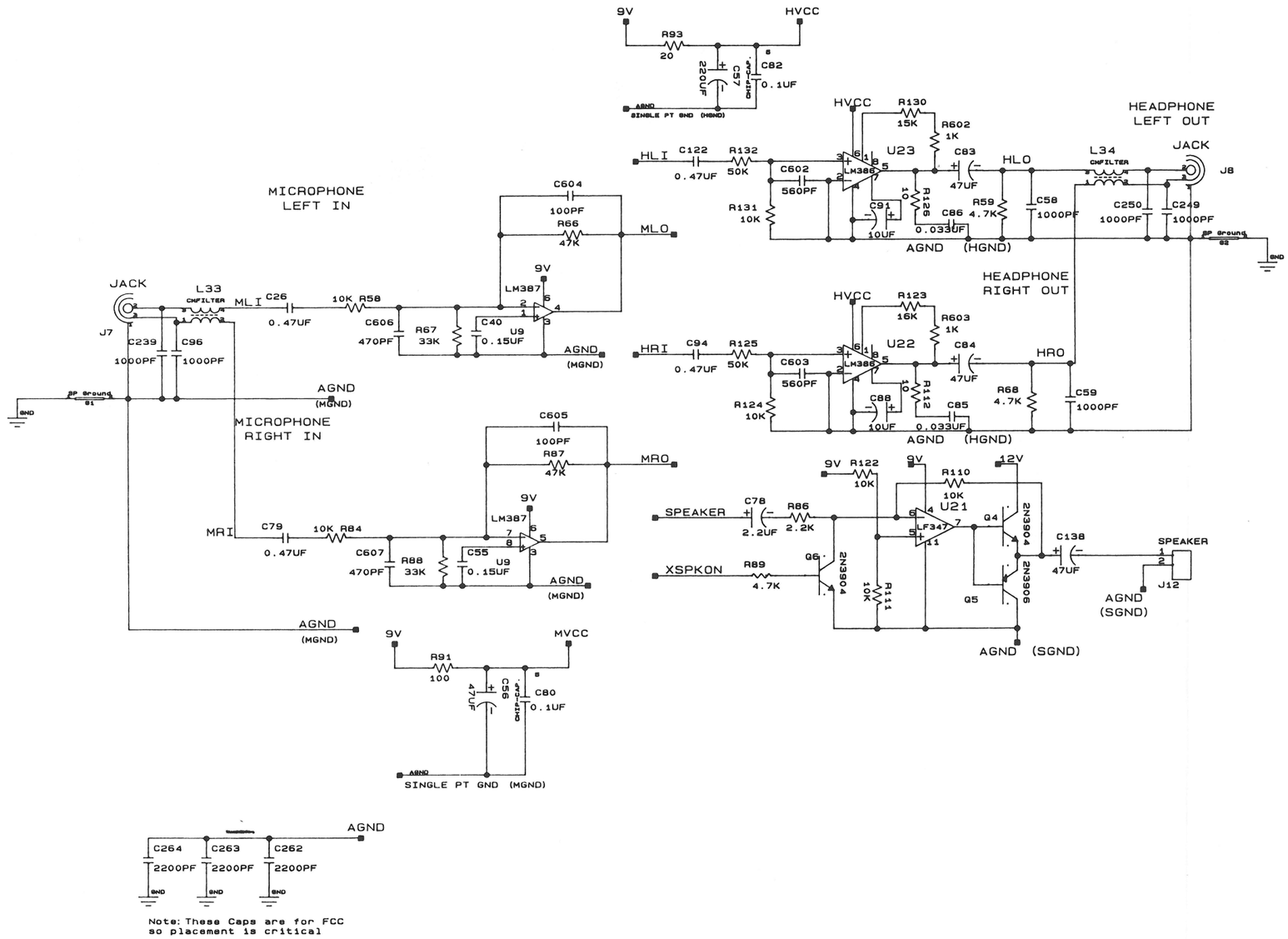
VEE

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1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

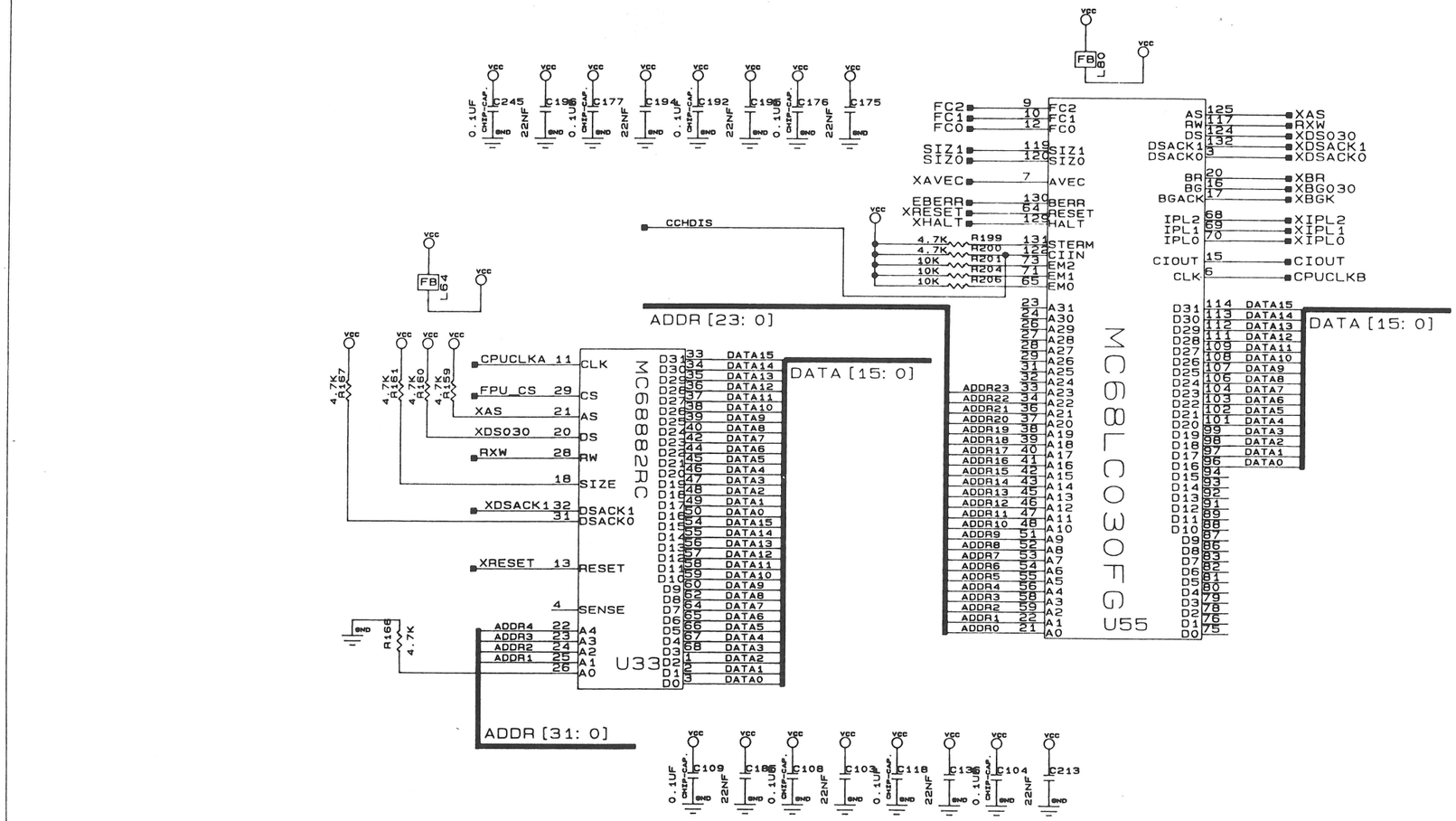
TITLE FALCON030 SCHEMATIC

SIZE	CODE	NUMBER	REV
D		500047-001	B

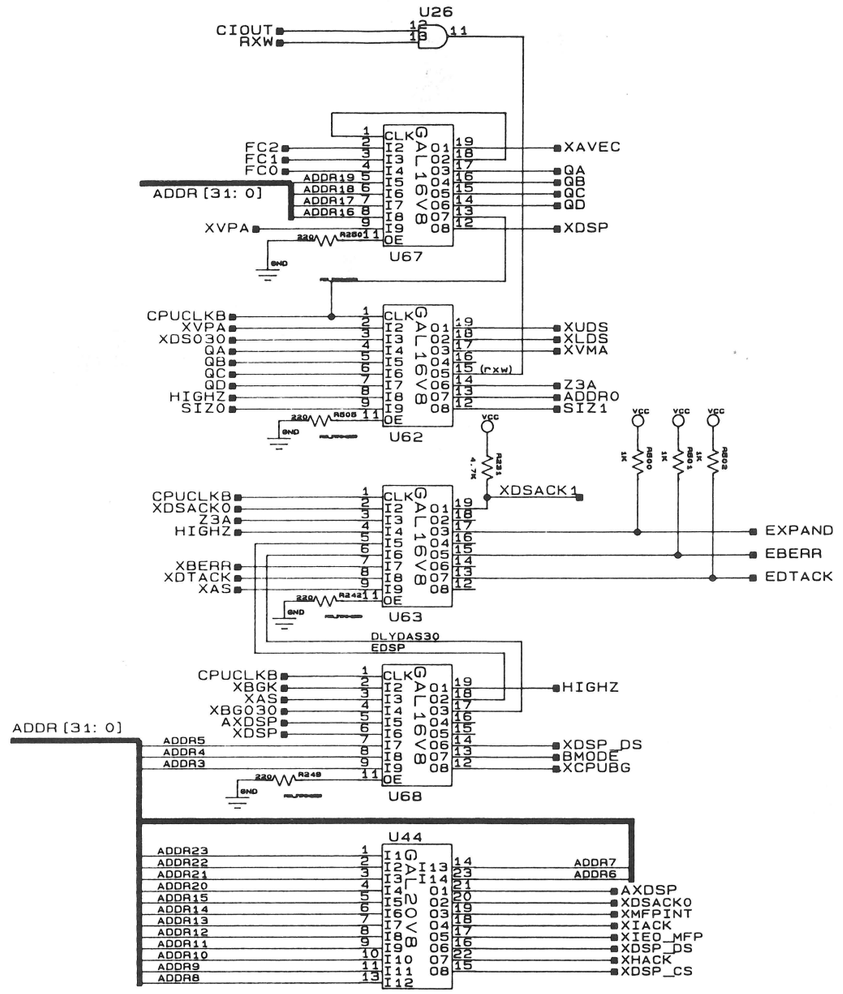
SHEET 10 OF 14



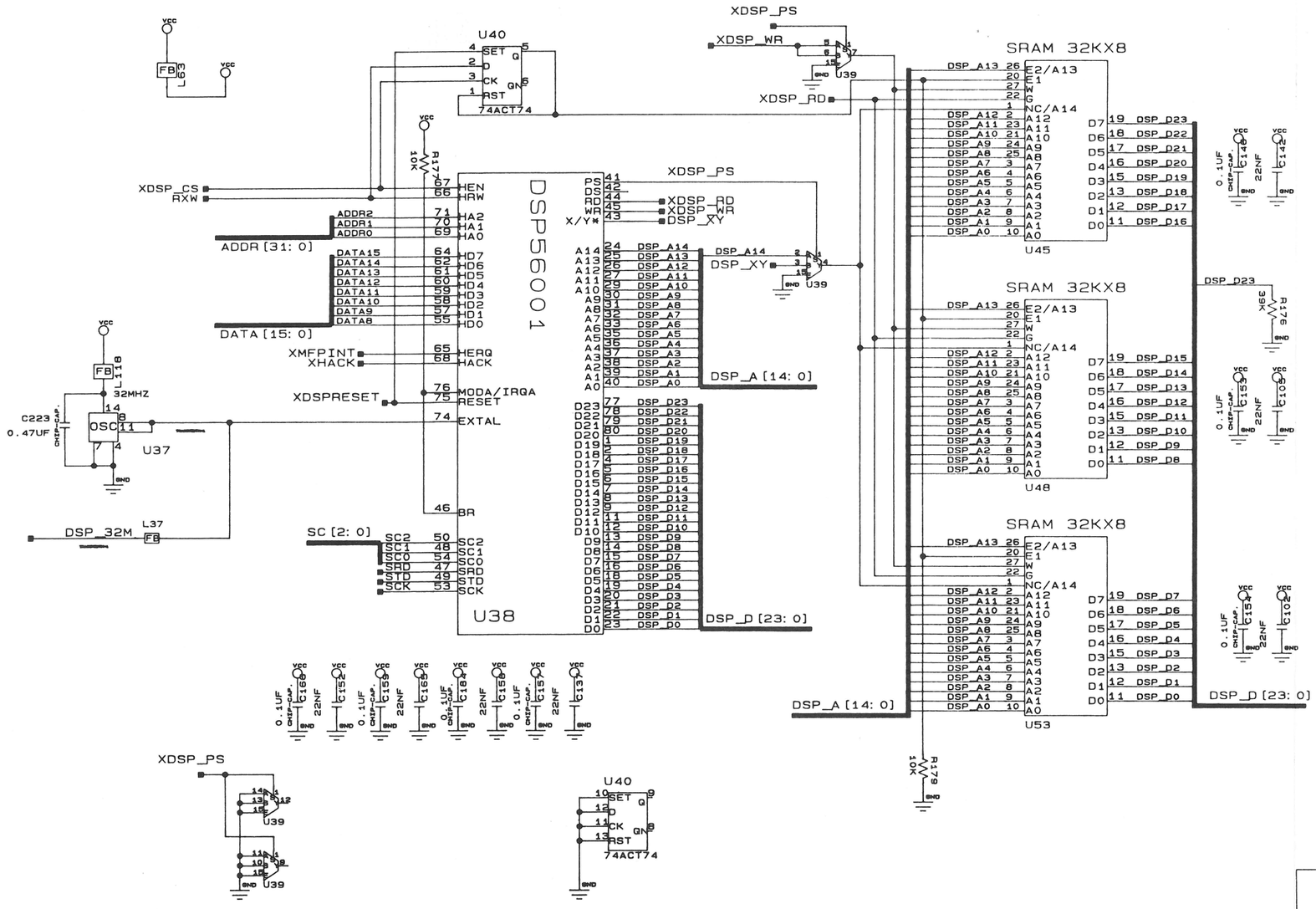
ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: 500047-001	REV: B
			SHEET 11 OF 14



ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: 500047-001	REV: B
			SHEET 12 OF 14



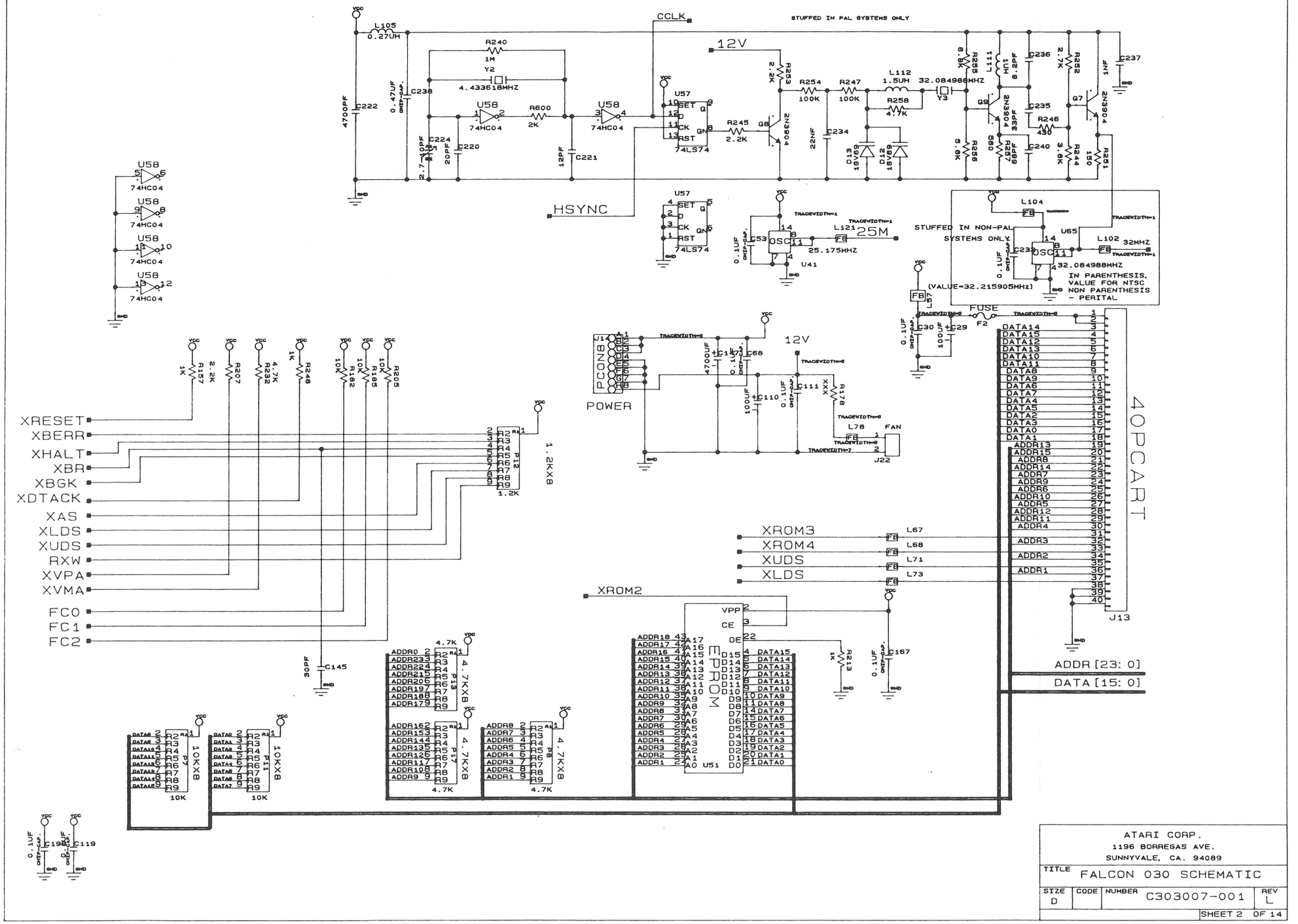
ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: 500047-001	REV: B
			SHEET 13 OF 14



ATARI CORP.		
1196 BORREGAS AVE.		
SUNNYVALE, CA. 94089		
TITLE: FALCON030 SCHEMATIC		
SIZE: D	CODE:	NUMBER: 500047-001 REV: B
		SHEET 14 OF 14

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	7/23/92	
B	REVISED PER ECO #1488	8/25/92	
C	REVISED PER ECO #1492	8/25/92	
D	REVISED PER ECO #1497	8/25/92	
E	REVISED PER ECO #1498		
F	REVISED PER ECO #1505	9/10/92	
G	REVISED PER ECO #1600	1/6/93	
H	REVISED PER ECO #1604	1/20/93	
J	REVISED PER ECO #1642	6/11/93	
K	REVISED PER ECO #1643	8/06/93	
L	REVISED PER ECO #1641	8/06/93	

		DRAWN BY TRH DATE	ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089
		CHECKED DATE	
CA401332		ENGINEER DATE	TITLE FALCON 030 SCHEMATIC
NEXT ASSEMBLY	USED ON ORIGINAL MODEL	APPROVED DATE	SIZE D / CODE / NUMBER C303007-001 / REV L
APPLICATION		APPROVED DATE	SHEET 1 OF 14



ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE	FALCON 030 SCHEMATIC		
SIZE D	CODE	NUMBER C303007-001	REV L
			SHEET 2 OF 14

* - OPTIONAL COMPONENTS

ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE: FALCON 030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: C303007-001	REV: L
			SHEET 3 OF 14

FOR NON MODULATOR SYSTEMS ONLY

HSYNC
VSYNC
AVGND
COLOR
CCLK
REMOVE FOR PAL
MC1377
U18
AUDIO
1HSYNC
3ESYNC
JMP3
W10

* - REQUIRES VALUE CHANGE FOR PAL

FOR MODULATOR SYSTEMS ONLY

NOTE: JMP2_ST MUST BE PLACED NEAR U35

32MHZ R234 22 CLK32
R241 22 VID32MHZ

VER_INT
WDATV
RDATV
HINTC
VREQC
RAMHV

U4 STMOD

COMBEL U56

DATA [15: 0]
ADDR [23: 0]
MADDR [10: 0]
XDTACK

VIDEL U34

SGC DAC U30

MDATA [15: 0]
MDATA [31: 16]

AVCC
DOTCK
ICLK
ROUT
GOUT
BOUT
RCON
GCON
BCON

SINGLE POINT GROUND

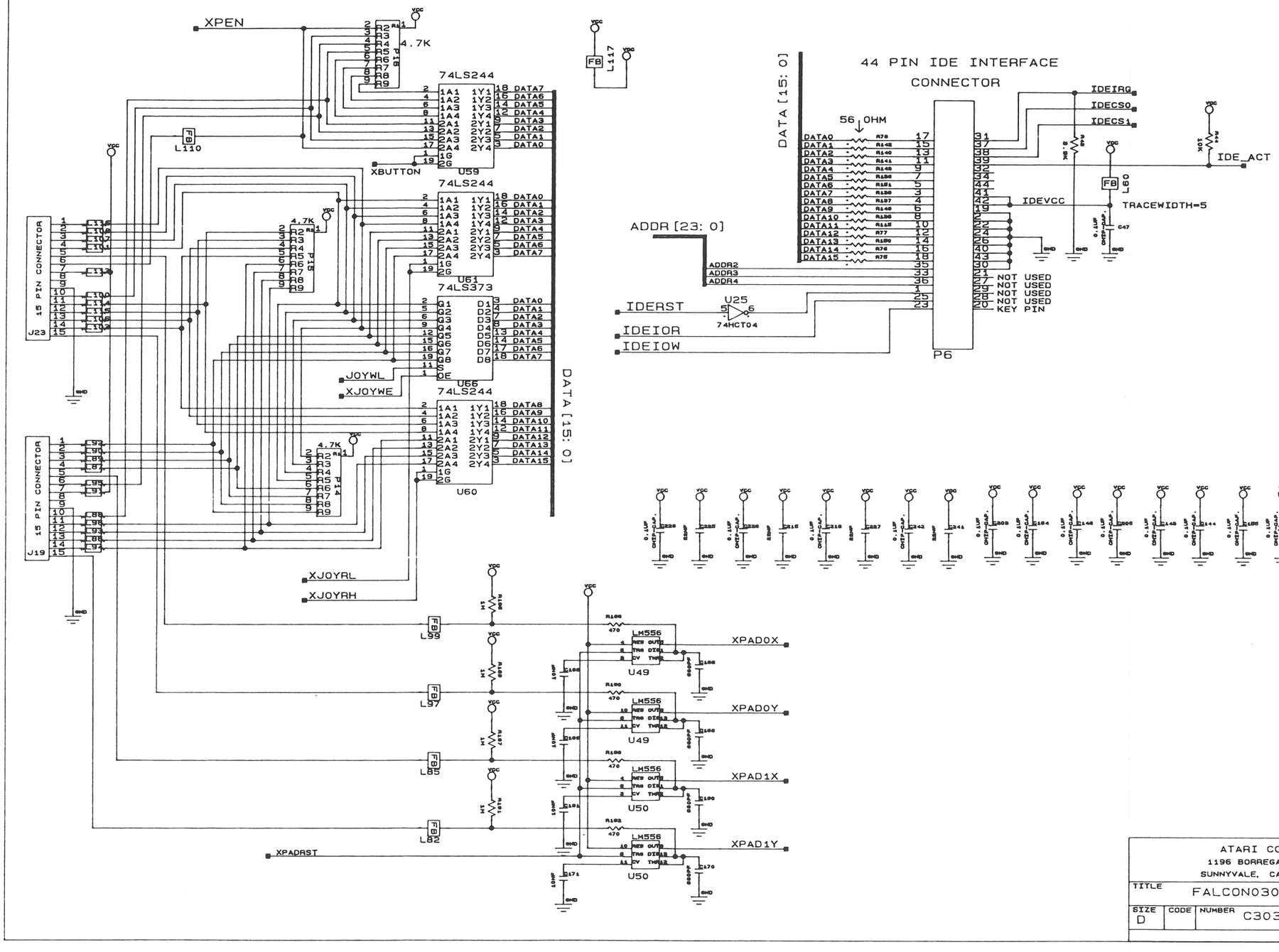
18 PIN VIDEO CONNECTOR J5

ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

TITLE: FALCON030 SCHEMATIC

SIZE	CODE	NUMBER	REV
D		C303007-001	L

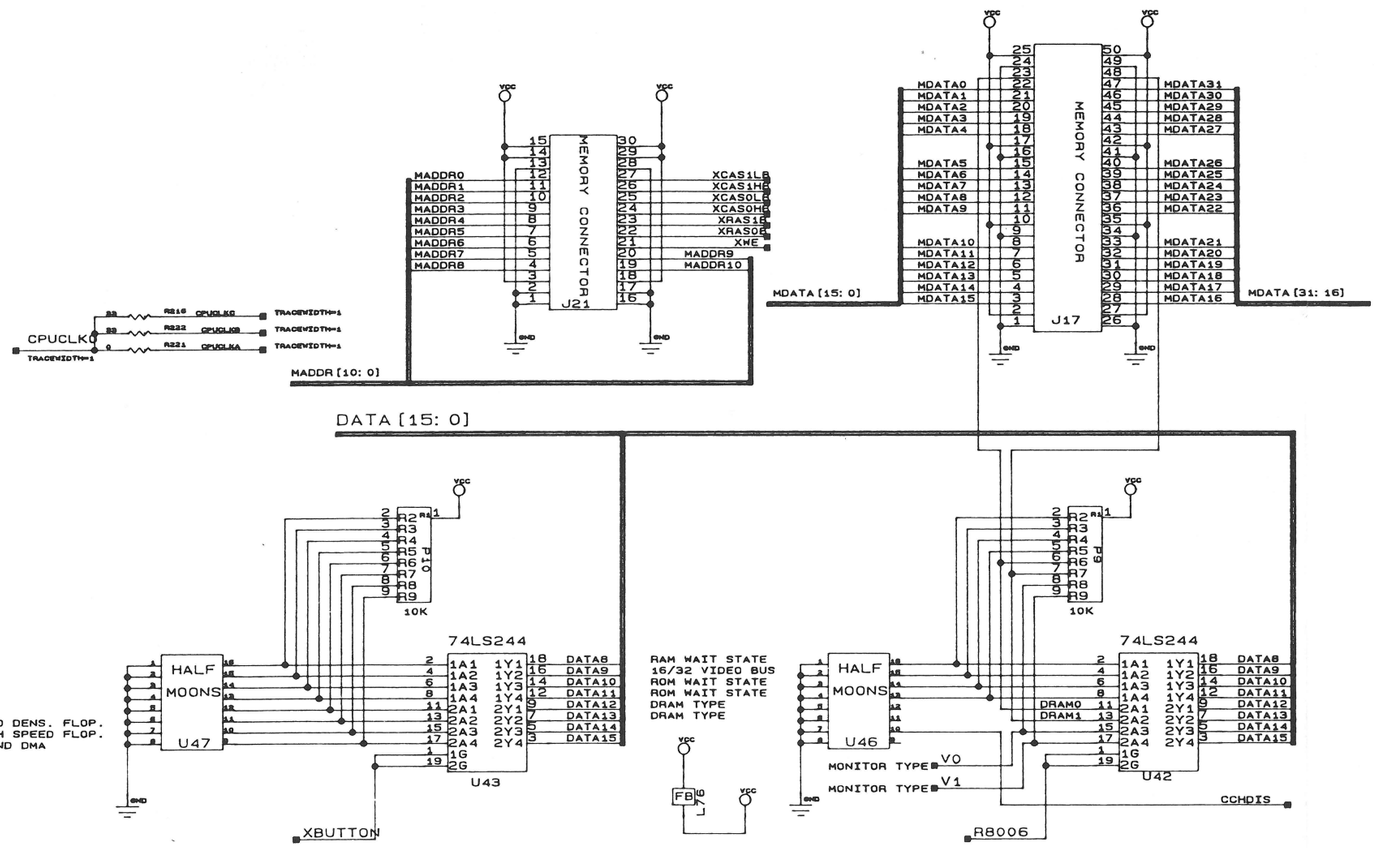
SHEET 4 OF 14



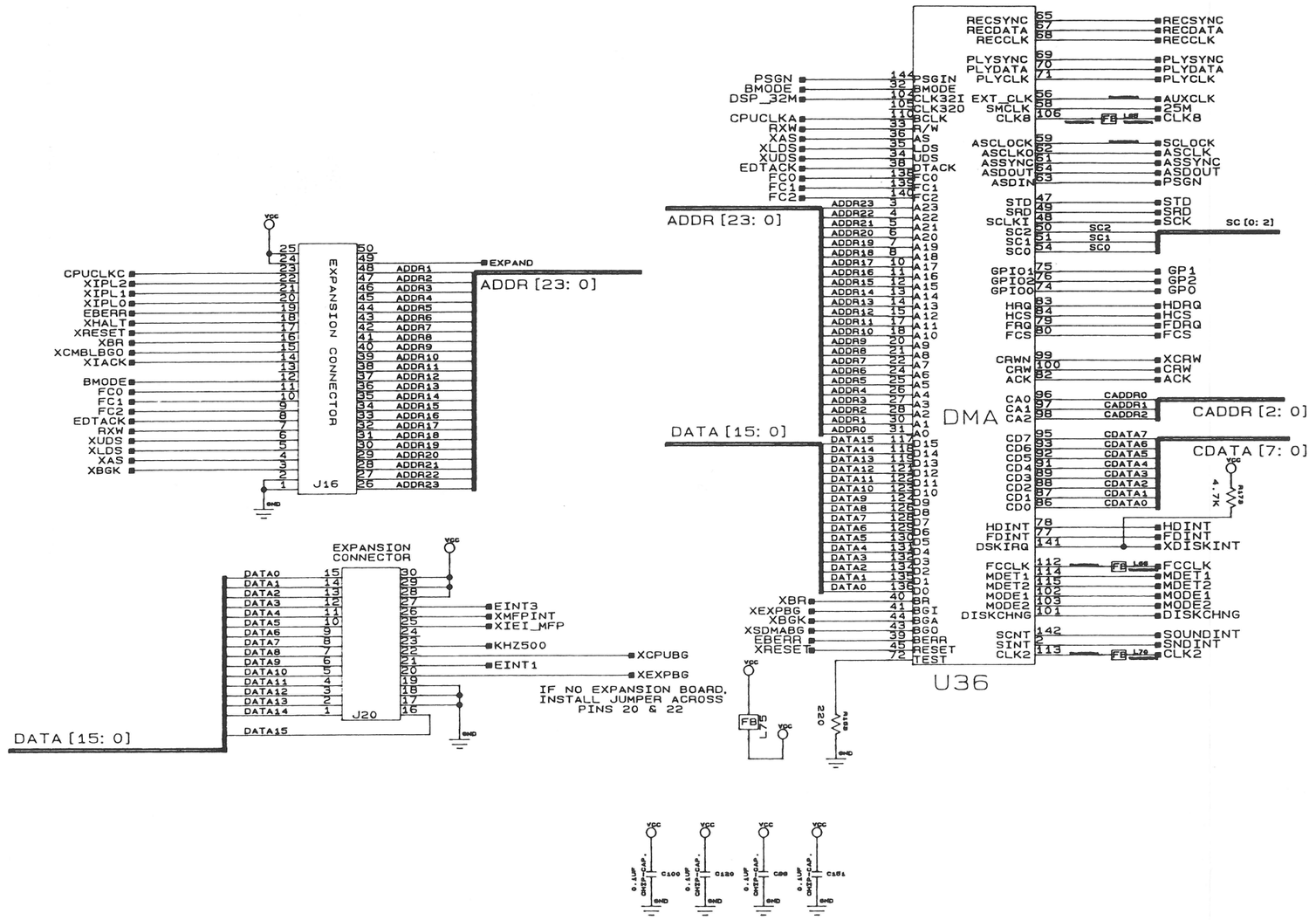
ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		C303007-001	L

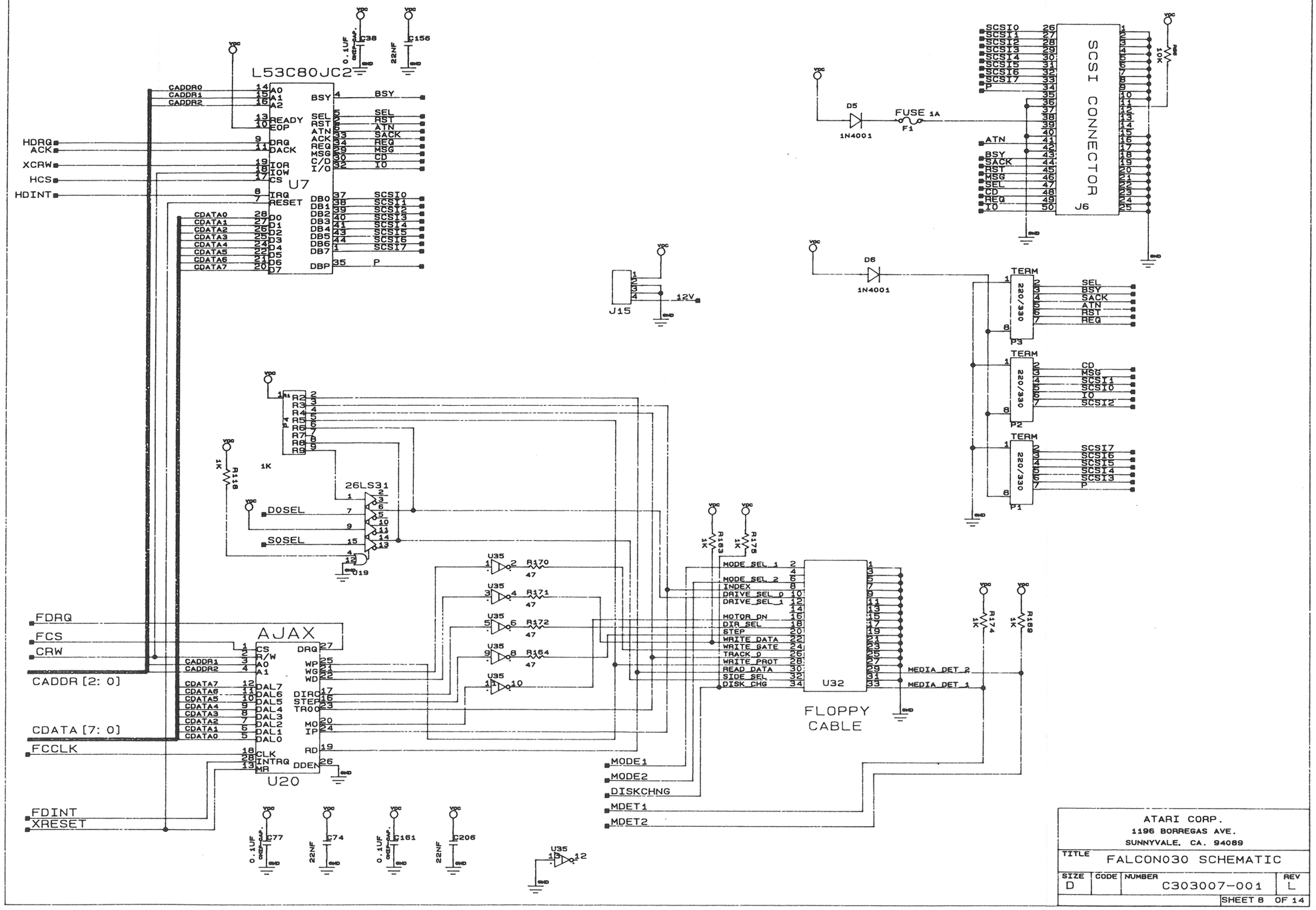
SHEET 5 OF 14



ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: C303007-001	REV: L
			SHEET 6 OF 14

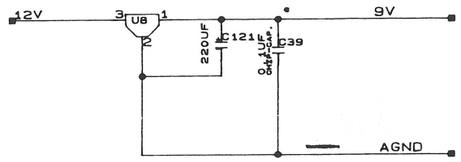


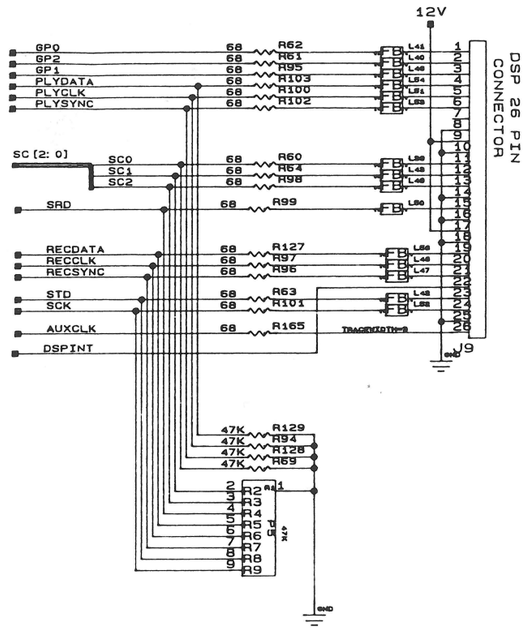
ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: C303007-001	REV: L
			SHEET 7 OF 14



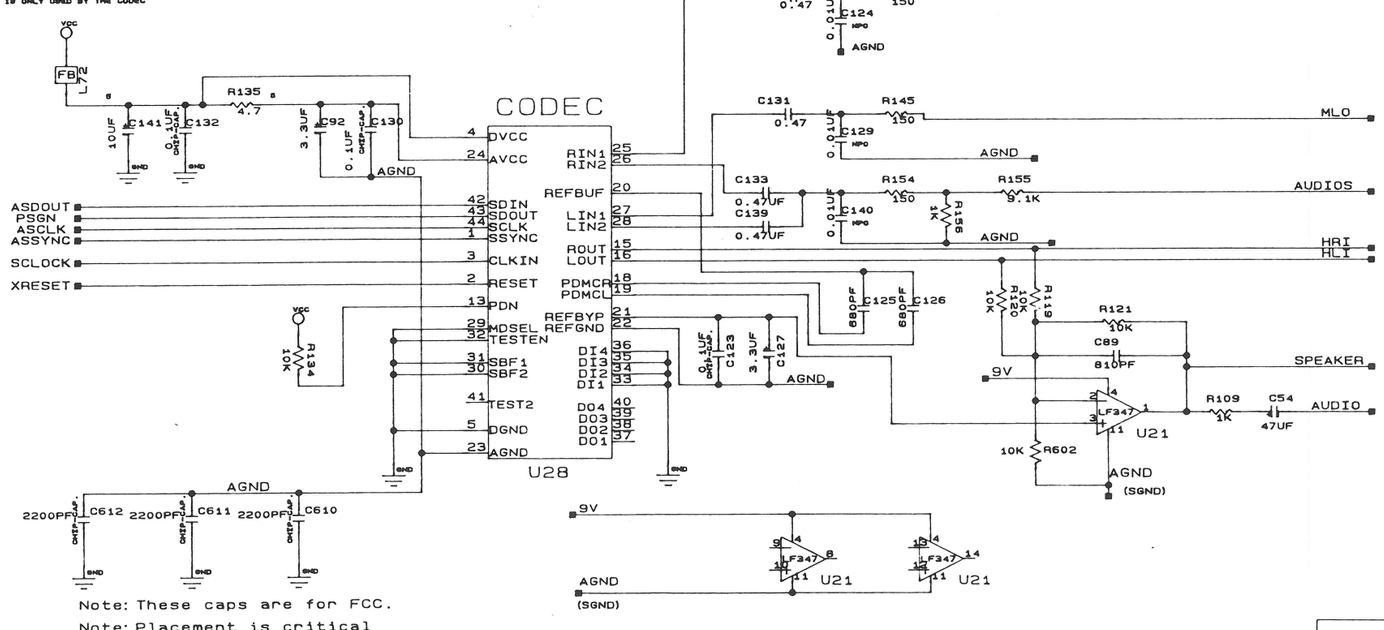
ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		C303007-001	L
		SHEET 8 OF 14	



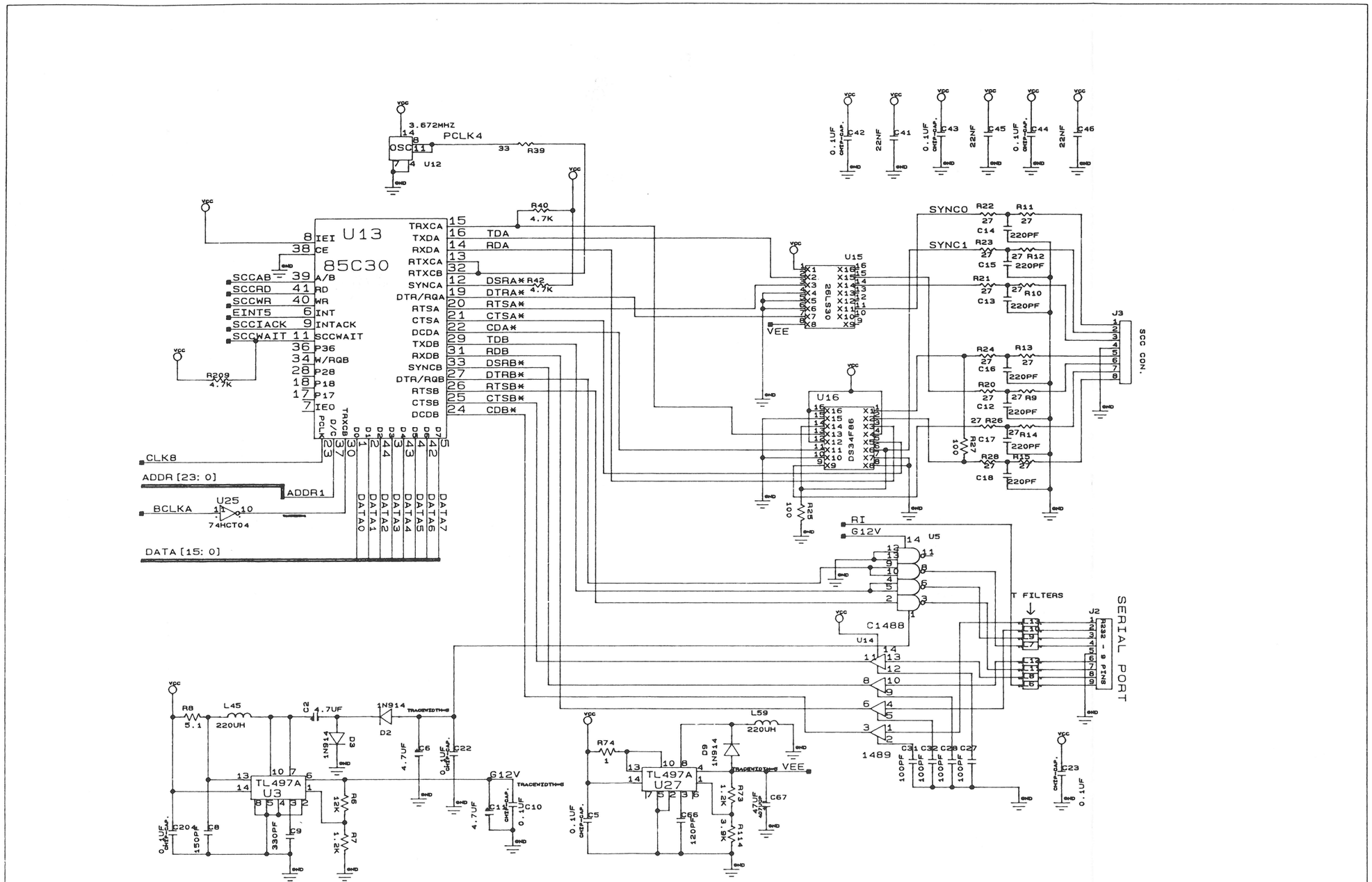


CLOCK TRACES, PARTICULARLY SCLOCK, SMCLK, AUXCLK MUST BE IDEAL WITH AS FEW TURNS/FEEDTHROUGHS AS POSSIBLE
USE CURVED TRACES IF POSSIBLE
KEEP TRACE WIDTH CONSTANT IF NOT. THEN TAPER SIGNALS TO AVOID SUDDEN IMPEDANCE CHANGES
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USE THE CERAMIC BEAD TO ISOLATE THE ISOLATION GAP BETWEEN THE SYSTEM AND AUDIO VCC AND GND PLANES
KEEP THE DVCC AND AVCC TRACES LOW IMPEDANCE USE WIDE TRACES AND 45 DEGREE ANGLES
USE THE INDICATED VCC TRACE IN THIS AREA TO CARRY THE +9V POWER AVCC IS ONLY USED BY THE CODEC



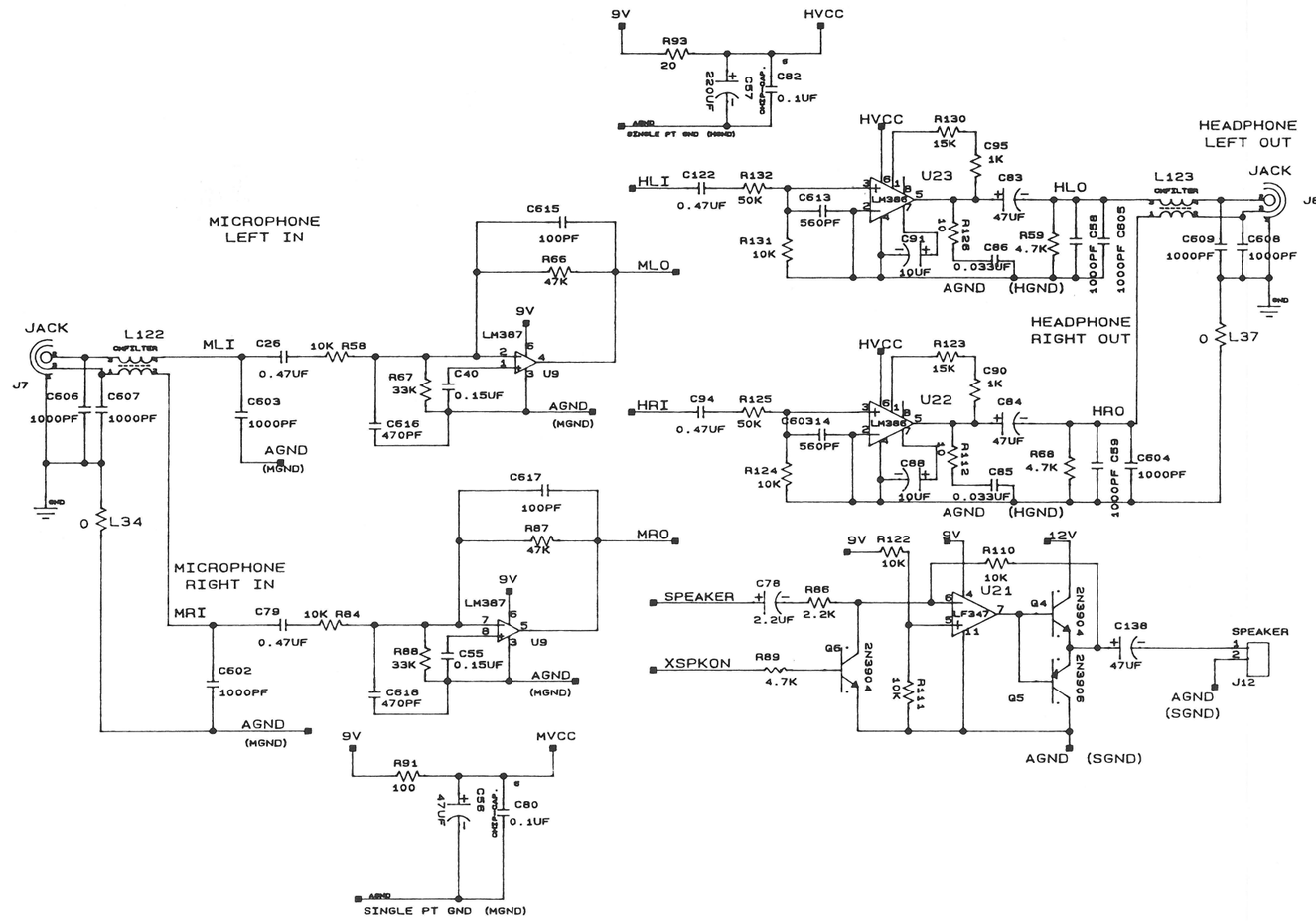
Note: These caps are for FCC.
Note: Placement is critical

ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE FALCON030 SCHEMATIC			
SIZE D	CODE	NUMBER C303007-001	REV L
			SHEET 9 OF 14

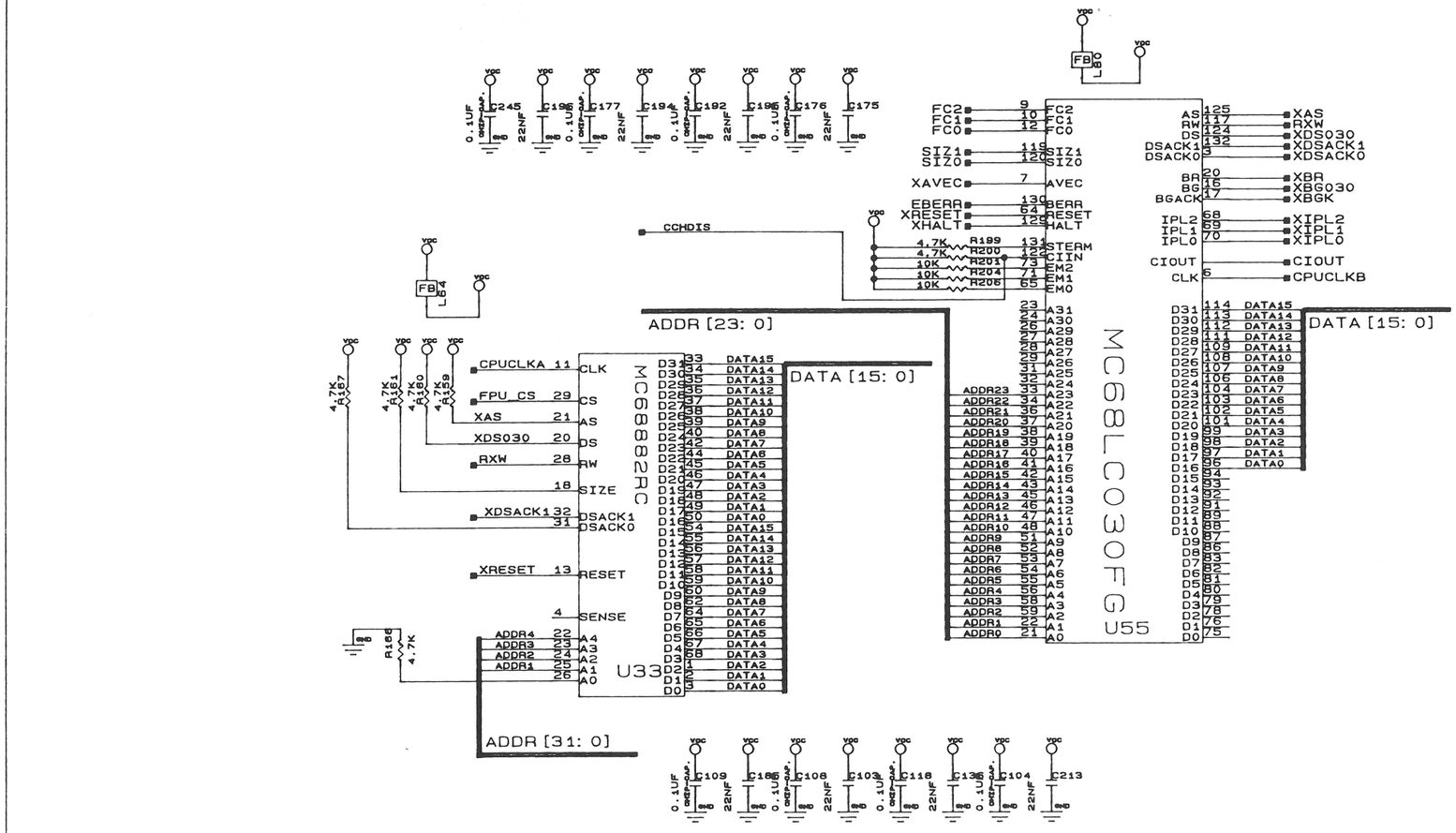


ATARI CORP.
1196 BORREGAS AVE.
SUNNYVALE, CA. 94089

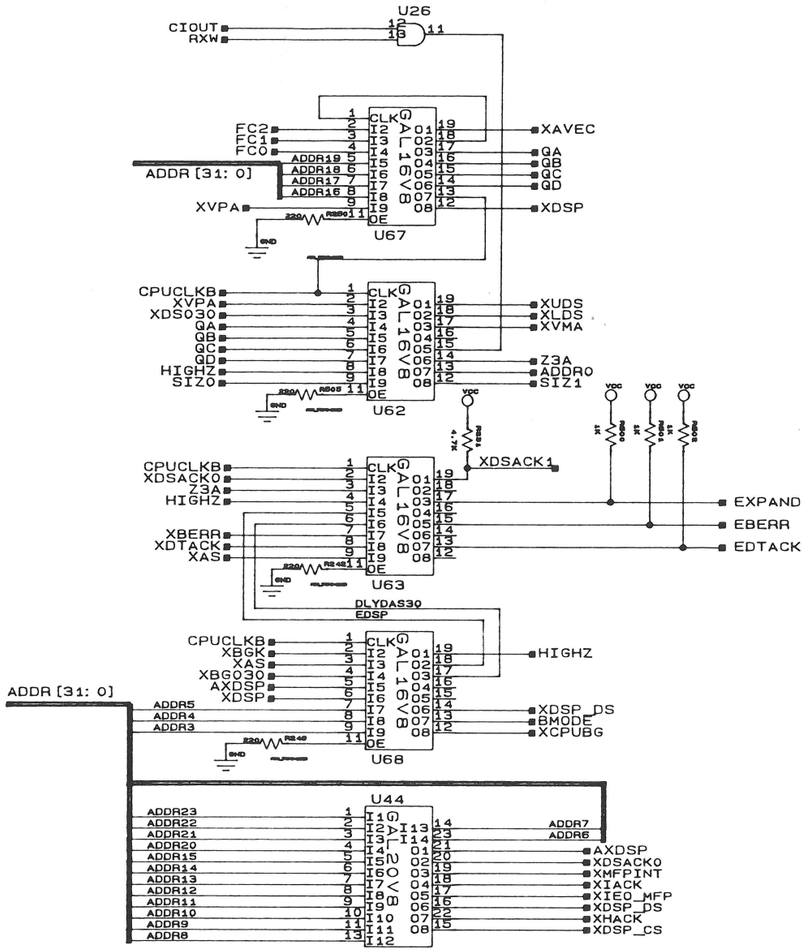
TITLE			
FALCON030 SCHEMATIC			
SIZE	CODE	NUMBER	REV
D		C303007-001	L
			SHEET 10 OF 14



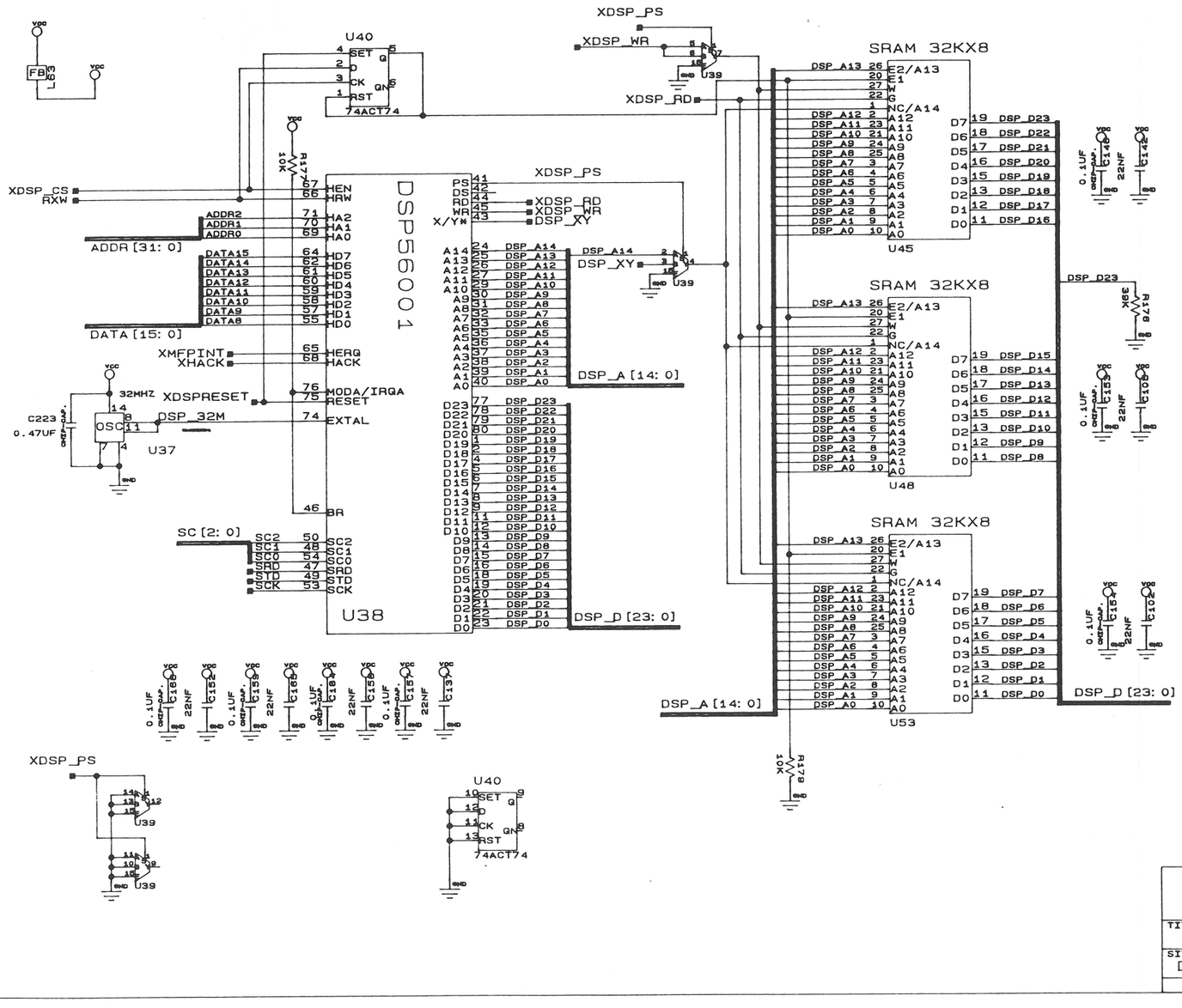
ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE	FALCON030 SCHEMATIC		
SIZE D	CODE	NUMBER C303007-001	REV L
			SHEET 11 OF 14



ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: C303007-001	REV: L
			SHEET 12 OF 14



ATARI CORP.			
1196 BORREGAS AVE.			
SUNNYVALE, CA. 94089			
TITLE	FALCON030 SCHEMATIC		
SIZE D	CODE	NUMBER C303007-001	REV L
			SHEET 13 OF 14



ATARI CORP. 1196 BORREGAS AVE. SUNNYVALE, CA. 94089			
TITLE: FALCON030 SCHEMATIC			
SIZE: D	CODE:	NUMBER: C303007-001	REV: L
			SHEET 14 OF 14